



H61H2-LM3

Rev : 1.0

ECS
CONFIDENTIAL

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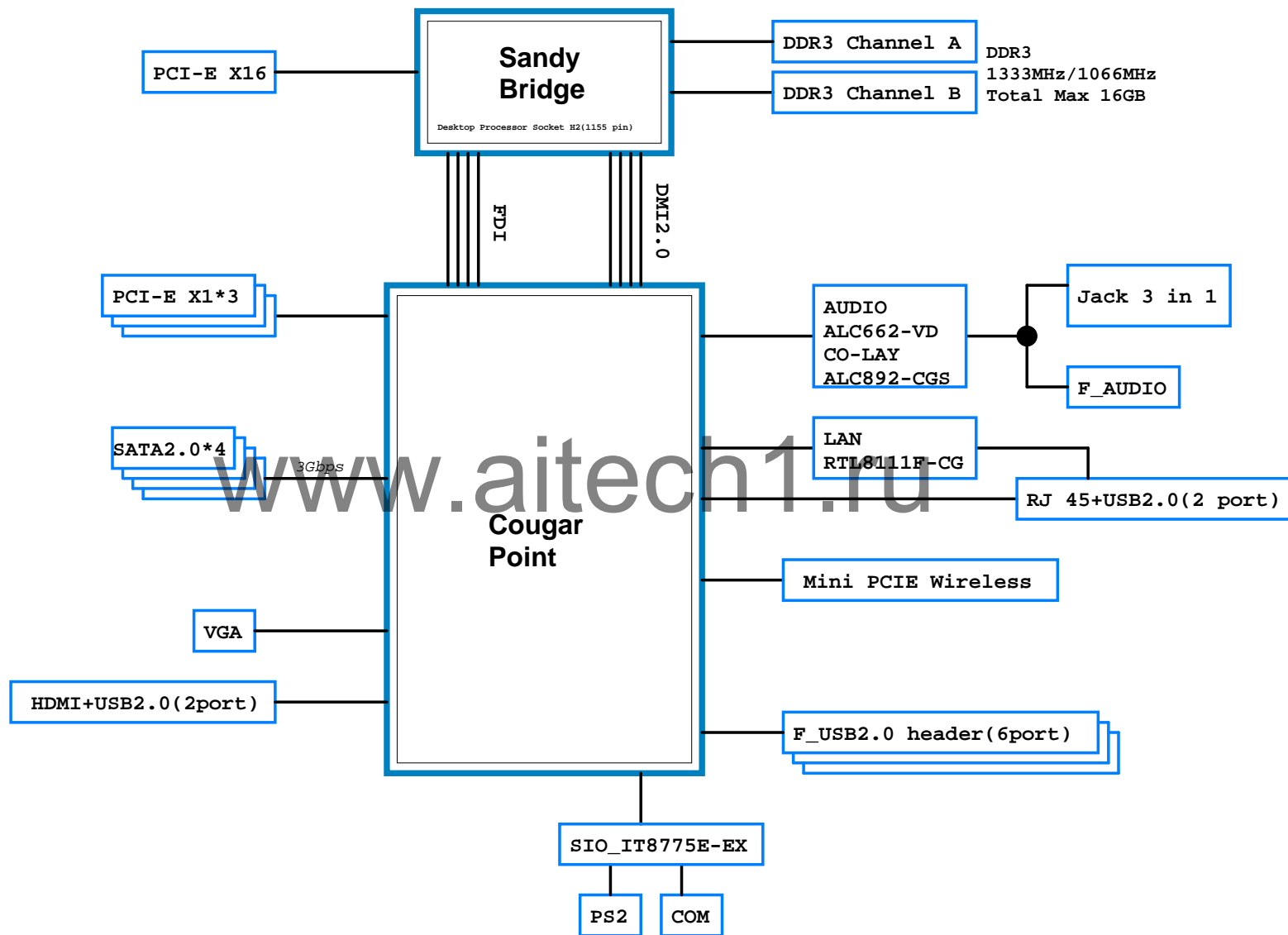
REVISION HISTORY:

Rev	Date	Notes
V0.1	11/06/29	
V0.2	11/07/29	1.CLK SI:R374=51 OHM,R376=51 OHM,R378=47 OHM,R425=47 OHM 2.VGA SI:R27=47 OHM,R28=47 OHM,R18=120 OHM,R20=120 OHM 3.DC SI:PFB3=0 OHM,ADD C289,DEL SC75 4.SPEC CHANGE:DEL USB_HDMI,ADD HDMI,ADD USBX2 5.COLAY ALC662-VC:ADD R102,EC88,U18,MN14,R781,D16,R780,R537,R542,R543 6.HDA SI:ADD R112 7.ADD DPWROK CIRCUIT:ADD R680,C656,MN15,R660,QN12,R646 8.ADD WIFI LED CIRCUIT:ADD D51,R655 9.VRM12 CHANGE:C463=470P,C231=2200P,C230=1500P,R254=6.49K,R272=11.5K,R162=3.01K, C240=1000P,C454=3300P,R294=93.1K 10.VRM 65W: R275=29.4K,R300=21.5K,R217=60.4K DEL:R225,C2220,R255,R217,R319,R898,R157,C159,R159,R148,C163,R149,R186,C119 C118,R167,C171,L5,QCH4,QCL4,QCL8 ADD:R229,R279,R370 11.WIFI LED:ADD D51,R655,C659

NOTE:

Design by
428971_Sugar Bay_PDG_Rev2.0
443554_Intel_6_Series_C200_Series_Chipset_EDS_rev2_1
428969_Sugar Bay_CRB_Rev1.1

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PCH-GPIO function


Pin Name	Power Well	Usage	Default Status
GPIO1	VCC3	GP1_BOMDET2	GPI
GPIO6	VCC3	GP6_BOMDET3	GPI
GPIO7	VCC3	GP7_BOMDET4	GPI
GPIO9	3VSB	WIFI_CTL	Native
GPIO10	3VSB	USB_OC_L6	Native
GPIO11	3VSB	SMBALERT_L	Native
GPIO12	3VSB	MODE_TRIGGER	Native
GPIO13	3VSB	LPC_PME	GPI
GPIO14	+DIMM_5VDUAL	PCH_LED1	Native
GPIO17	VCC3	GP17_BOMDET1	GPI
GPIO21	VCC3	GPIO21_COM2_DET	GPI
GPIO22	VCC3	CLR_CMOS_GP22	GPI
GPIO23	VCC3	LPC_DRQ1_L	Native
GPIO24	3VSB	PCH_SKTOCC_L	GPO
GPIO27	+PS_3VSB	MS_GP0	GPI
GPIO30	+PS_3VSB	SUSWARN_L	Native
GPIO31	+PS_3VSB	MS_GP1	GPI
GPIO39	VCC3	GPIO39_CASE0	GPI
GPIO40	3VSB	USB_OC_L1	Native
GPIO41	3VSB	USB_OC_L2	Native
GPIO42	3VSB	USB_OC_L3	Native
GPIO43	3VSB	USB_OC_L4	Native
GPIO45	3VSB	WLAN_DIS_L	Native
GPIO48	VCC3	GPIO48_CASE1	GPI
GPIO57	3VSB	MODE_CTRL	GPI
GPIO59	3VSB	USB_OC_L0	Native
GPIO63	3VSB	SLP5_L	Native
GPIO64	VCC3	LDG33M	Native
GPIO67	VCC3	SIO48M	Native
GPIO72	3VSB	GPIO72_BOMDET5	Native

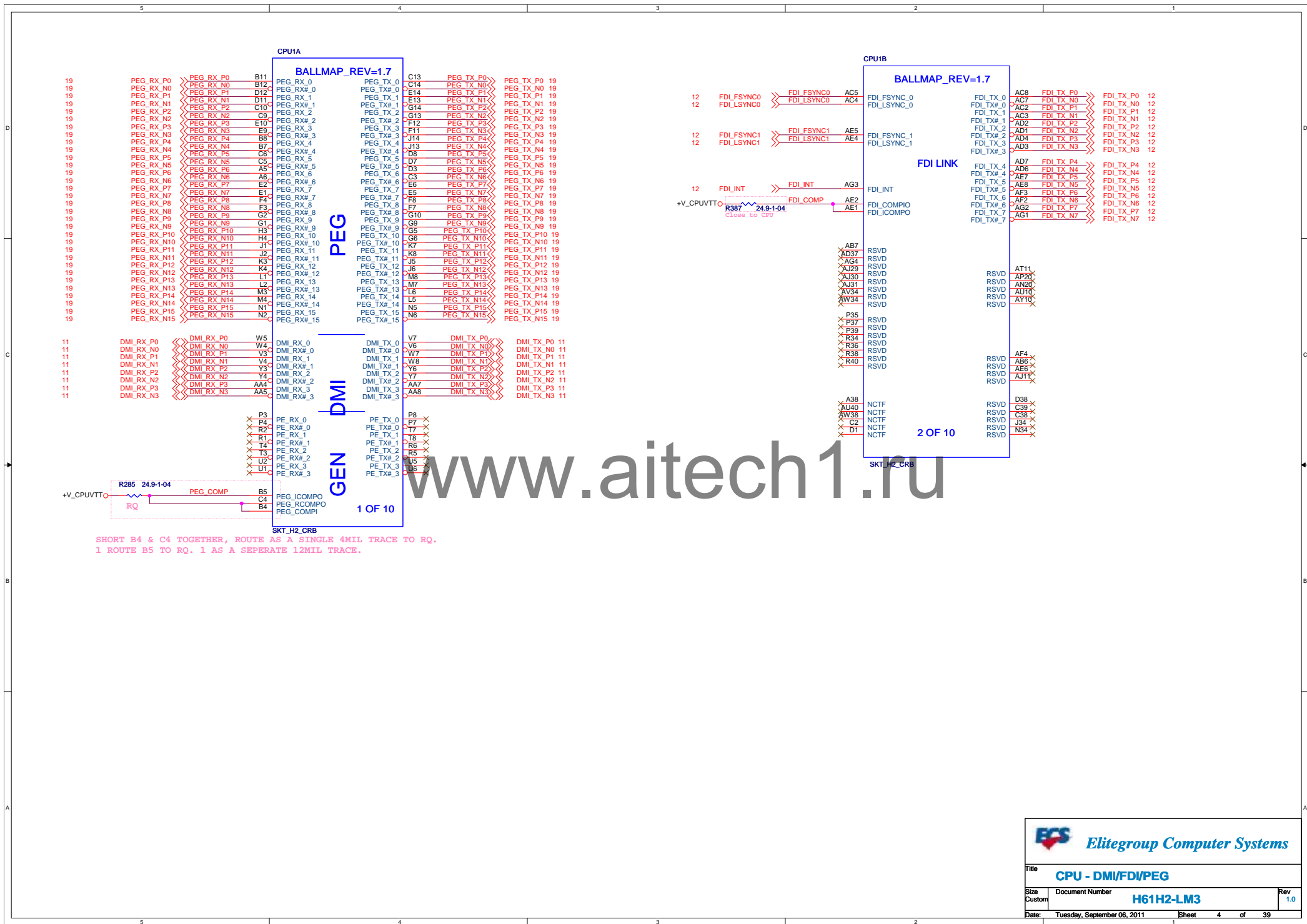
SIO-GPIO function

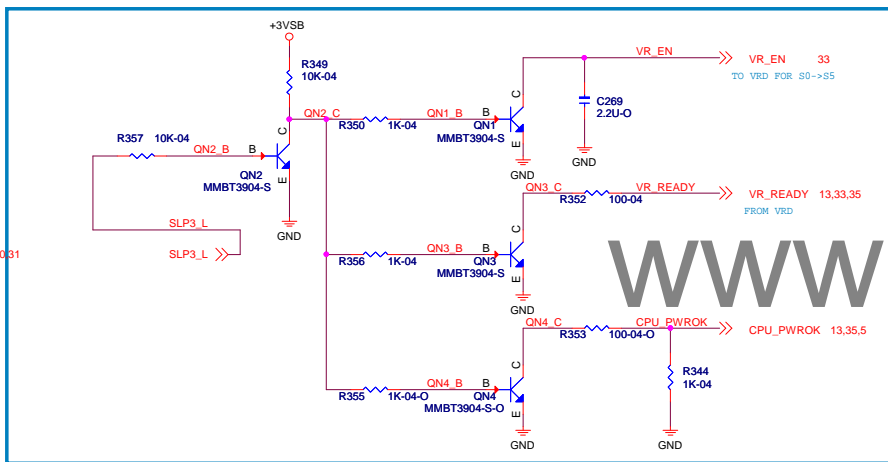
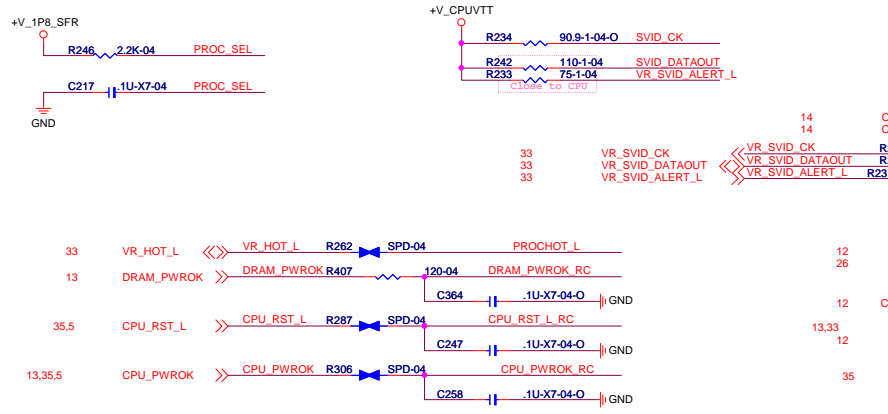
Pin Name	Power Well	Usage	Default Status
GP10	3VSB	SIO_PCIRST3_L	PCIRST3#
GP12	VCC3	SIO_PCIRST1_L	PCIRST1#
GP22	3VSB	SIO_LED0	GP22
GP23	3VSB	DPWROK	DPWROK
GP30	VCC3	ATXPWRGD	ATXPWRGD
GP31	VCC3	CTS1_L	CTS1#
GP32	VCC3	SIO_RI1_L	RI1#
GP33	VCC3	DCD1_L	DCD1#
GP36	VCC3	FAN_CTL3	FAN_CTL3
GP37	VCC3	FAN_TAC3	FAN_TAC3
GP40	3VSB	GPIO40_S4S5	3VSB5W#
GP41	3VSB	SIN1	SIN1
GP42	3VSB	PSON_L	PSON#
GP43	3VSB	FP_PWRBTN_L	PANSWH#
GP44	3VSB	SIO_PWRBTN_L	PWRON#
GP45	VCC3	DSR1_L	DSR1#
GP51	VCC3	FAN_CTL2	FAN_CTL2
GP52	VCC3	FAN_TAC2	FAN_TAC2
GP53	3VSB	SLP4_L	SUSC#
GP54	3VSB	LPC_PME_L	PME#
GP55	3VSB	RSMRST_L	RSMRST#
GP56	3VSB	MCLK	MCLK
GP57	3VSB	MDATA	MDAT
GP60	3VSB	KCLK	KCLK
GP61	3VSB	KDATA	KDAT
GP62	VCC3	KBRST_L	KRST#

H61 fuction PCI INT#

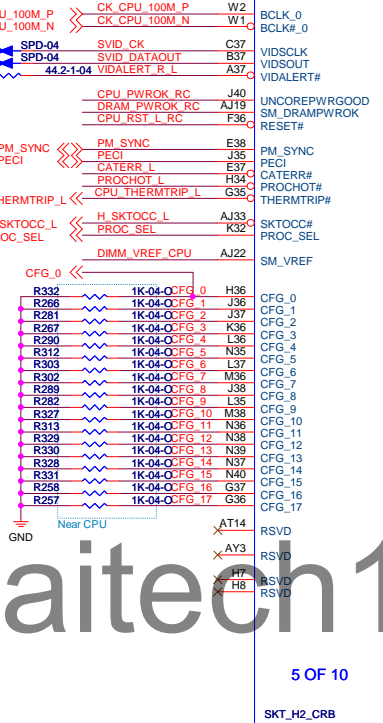
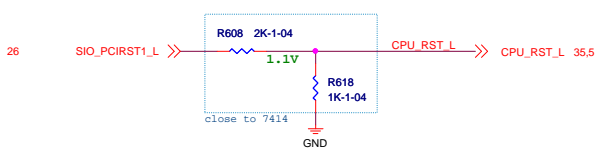
Function	INT PORT	PCIE 1X PORT	Chipset
LAN Controller	INT A#	PE_TX/RX_5	RTL8111F
PCIE1X_4 Wireless Card	INT C#	PE_TX/RX_3	H61 integrated
PCIE1X_1 Slot	INT D#	PE_TX/RX_4	H61 integrated
PCIE1X_2 Slot	INT B#	PE_TX/RX_6	H61 integrated
PCIE1X_3 Slot	INT B#	PE_TX/RX_2	H61 integrated
SATA Controller	INT B#	NA	H61 integrated

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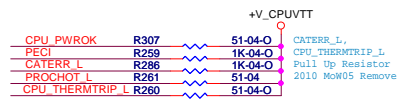
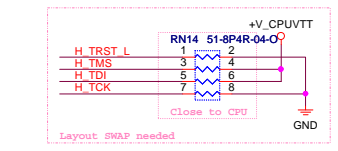
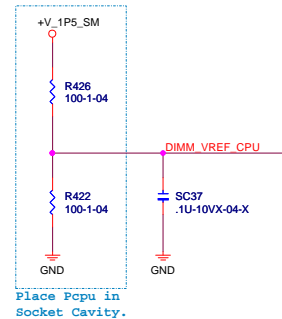




Power Down Sequencing Circuit



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CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1	CFG[5:6]
1 X 16	1	1	01=2X8,
2 X 8	0	1	10=RESERVED, 00=X8,X4,X4

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Title: **CPU - MISC**

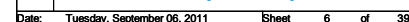
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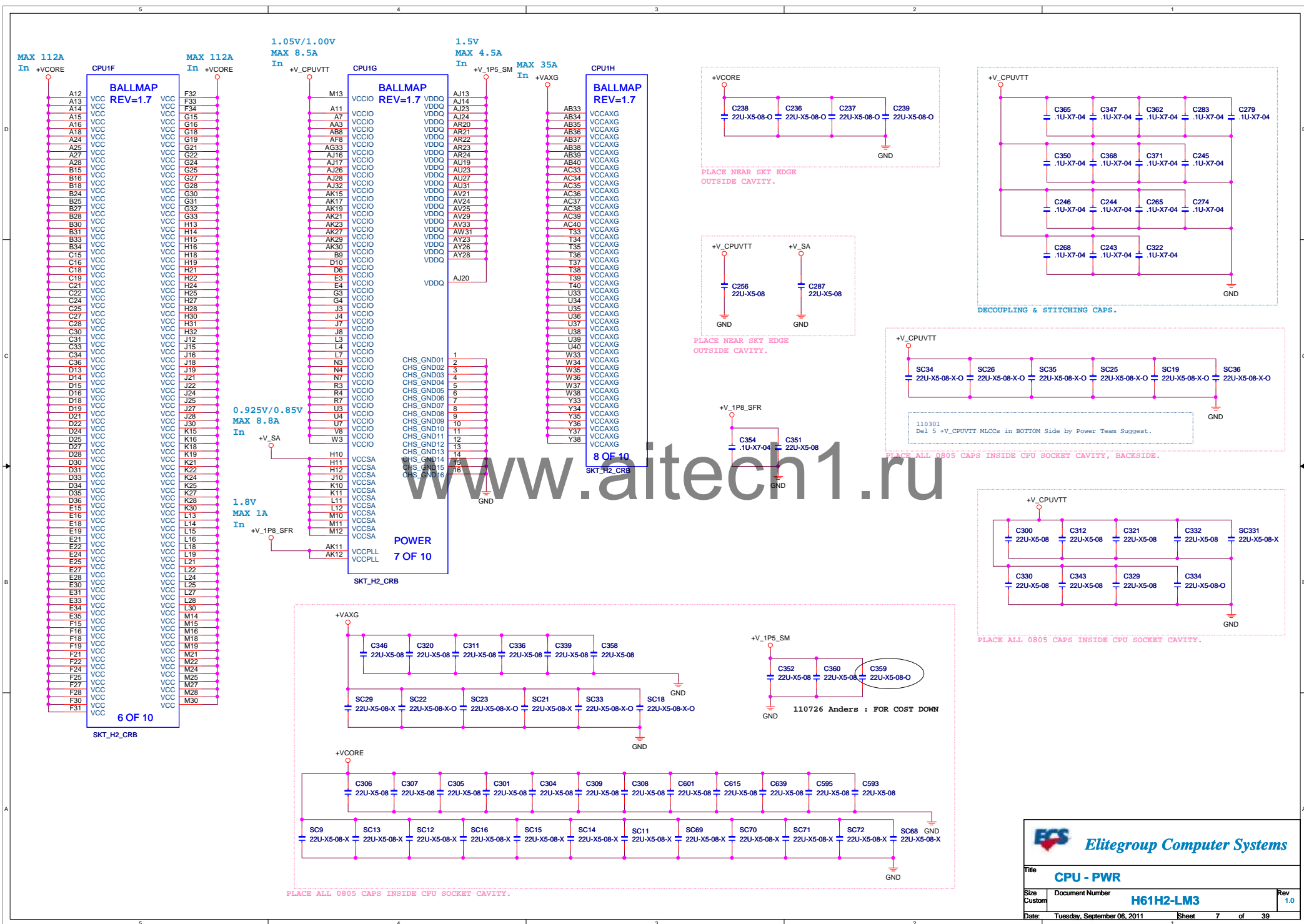
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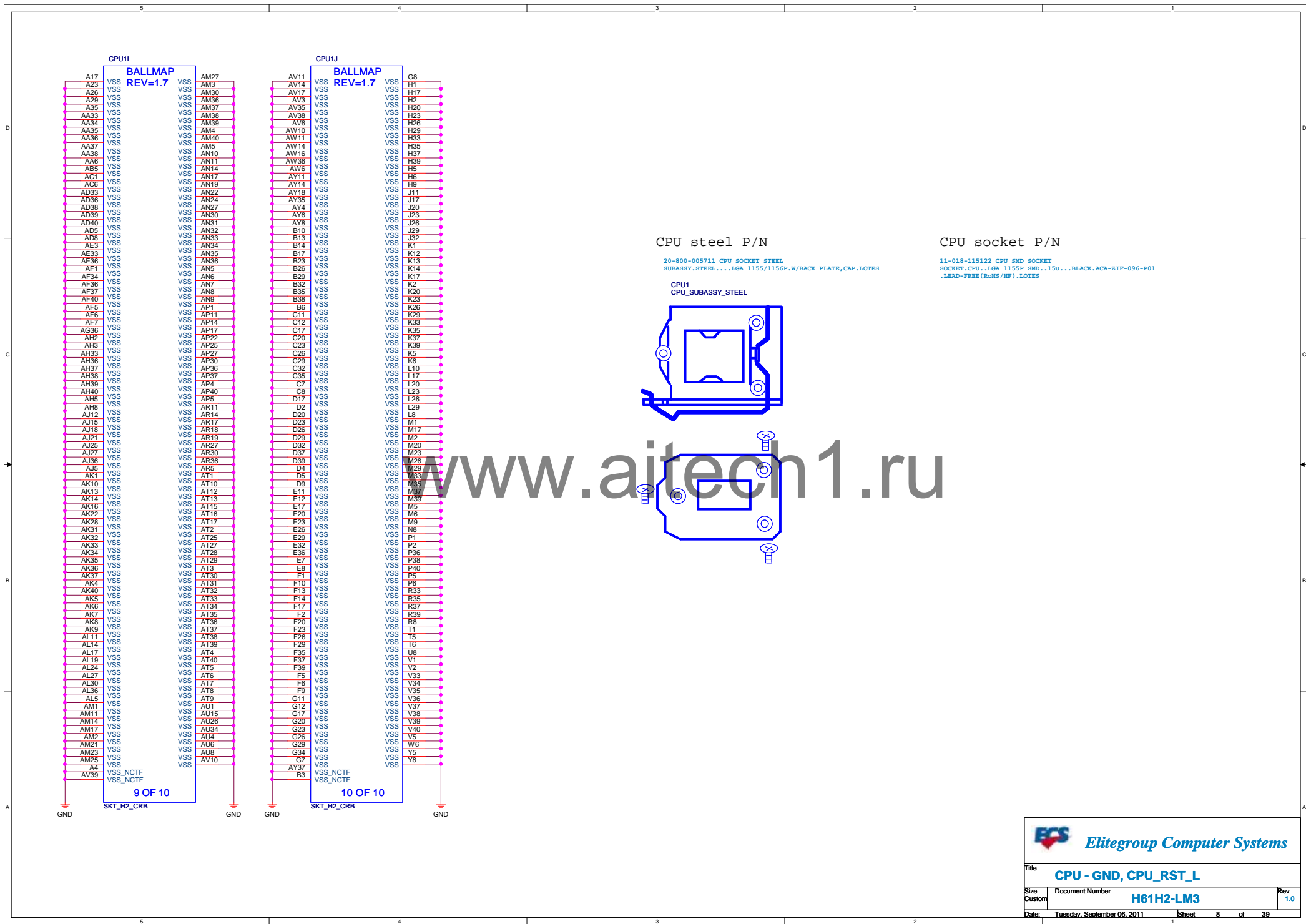
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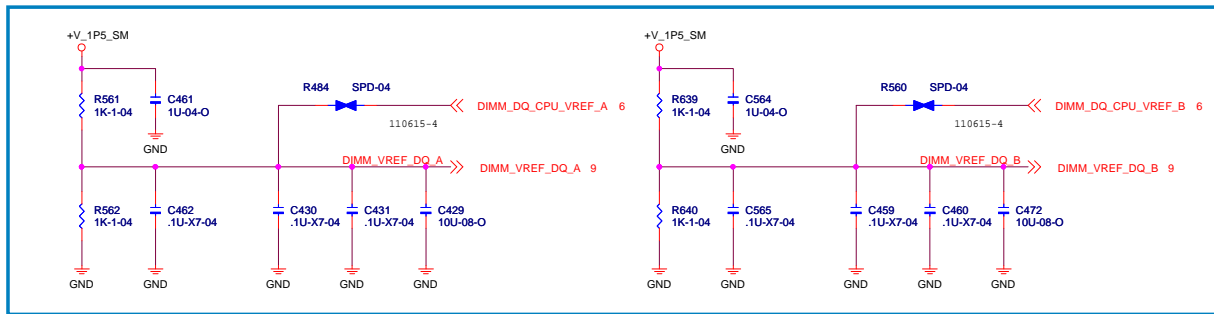
Sheet: **5** of **39**

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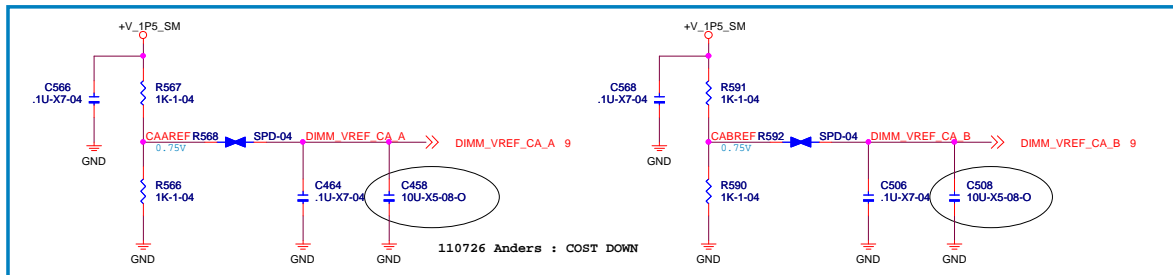




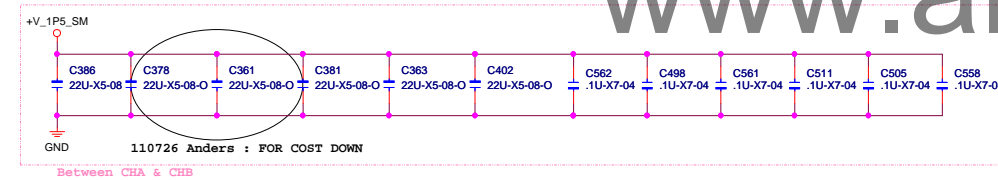




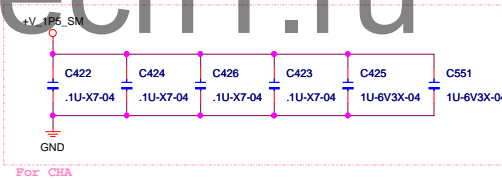
DIMM_VREF_DQ Control Circuit



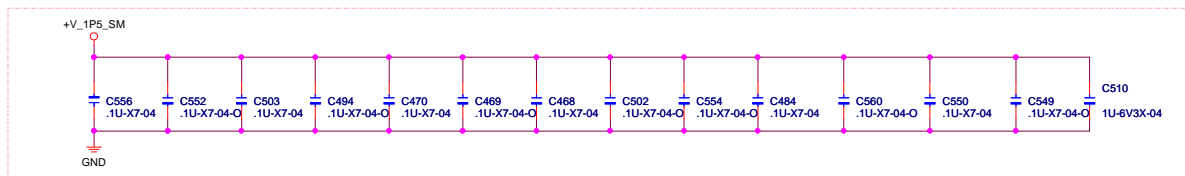
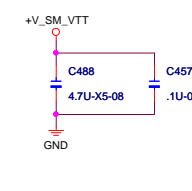
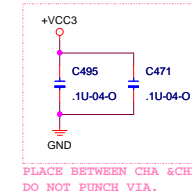
DIMM_VREF_CA Circuit



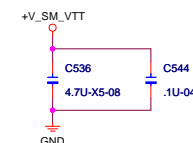
Between CHA & CHB

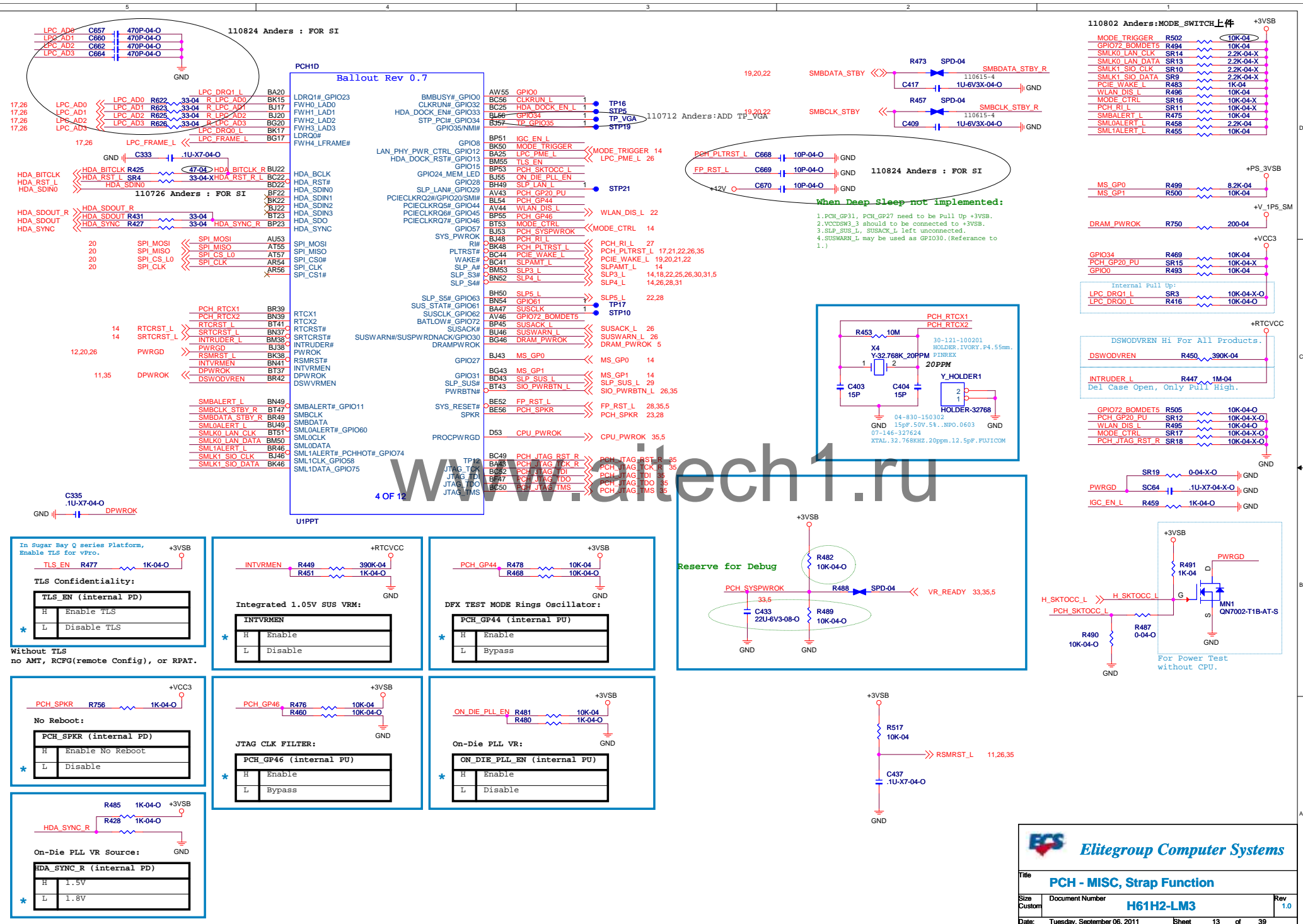


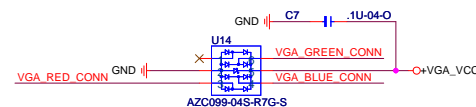
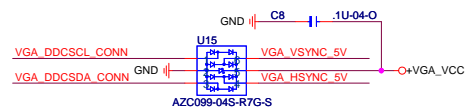
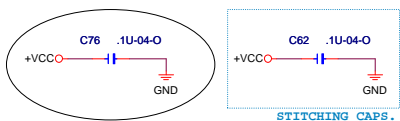
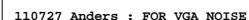
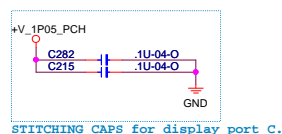
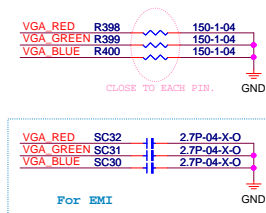
For CHA

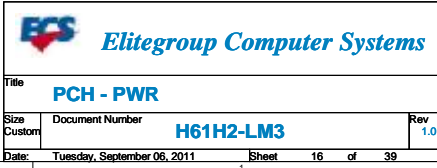


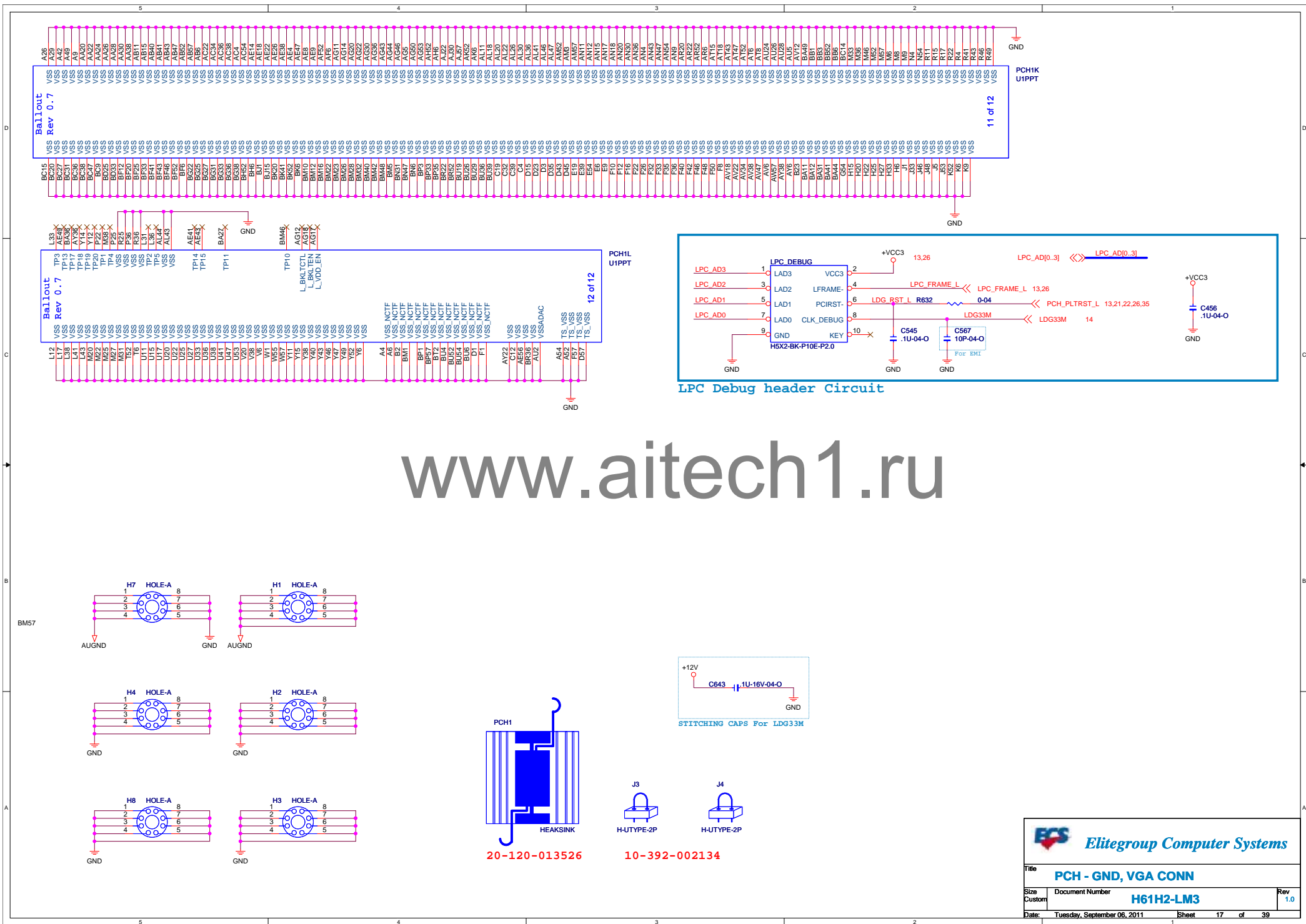
STITCHING CAPS FOR CMD, ADDR, CTL, BELOW CHBD3.

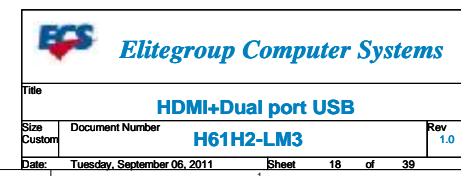












PCI-E SPEC:
VCC3-->3A
12V-->5.5A
3VSB-->0.375A

SMBCLK_STBY
SMBDATA_STBY

PCIE_WAKE_L

PCIE16X

KEY

RSVD_A

REFCLK_+H

REFCLK_-L

HSOP0_H

HSOP0_L

HSOP0_H

HSOP0_L

HSOP0_H

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HSOP0_L

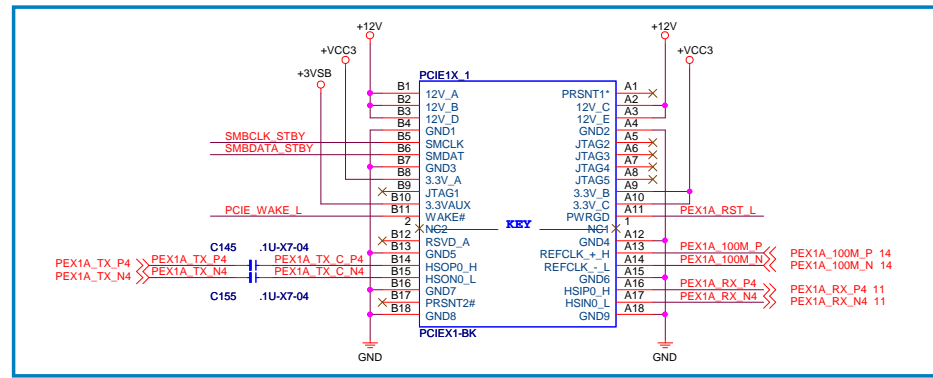
HSOP0_H

HSOP0_L

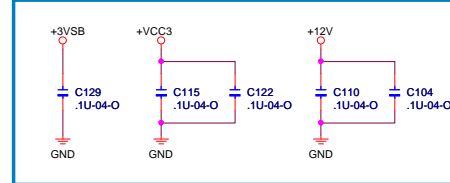
HSOP0_H

HSOP0_L

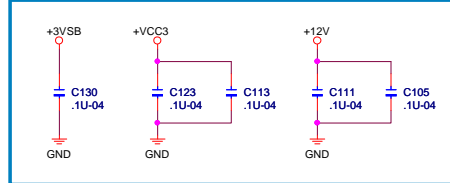
HSOP0_H



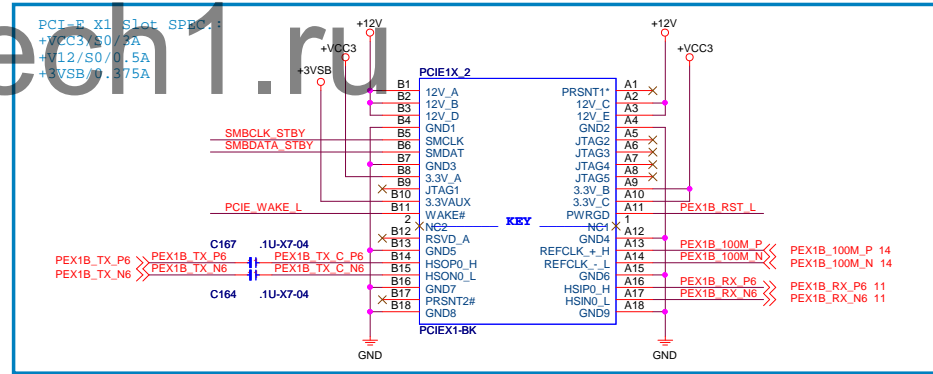
PCI-E X1 A



PCI-E X1 A Decoupling Cap.

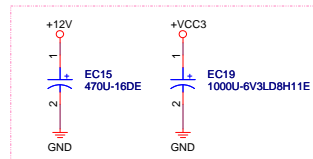


PCI-E X1 B Decoupling Cap.



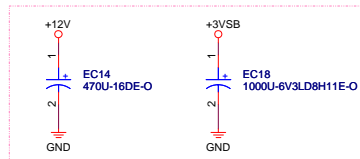
PCI-E X1 B

04-711-102073
E/C.1000uF.16V.20%...105C.RT D10*17mm....

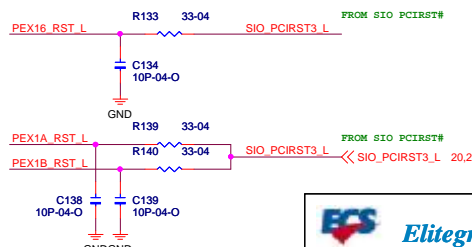


Between PEX16 & PEX1A

04-711-102073
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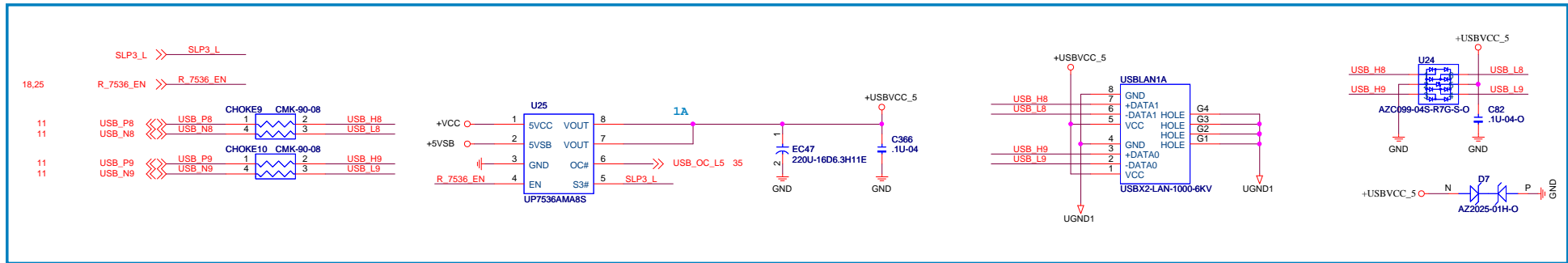


Between PEX1A & PEX1B

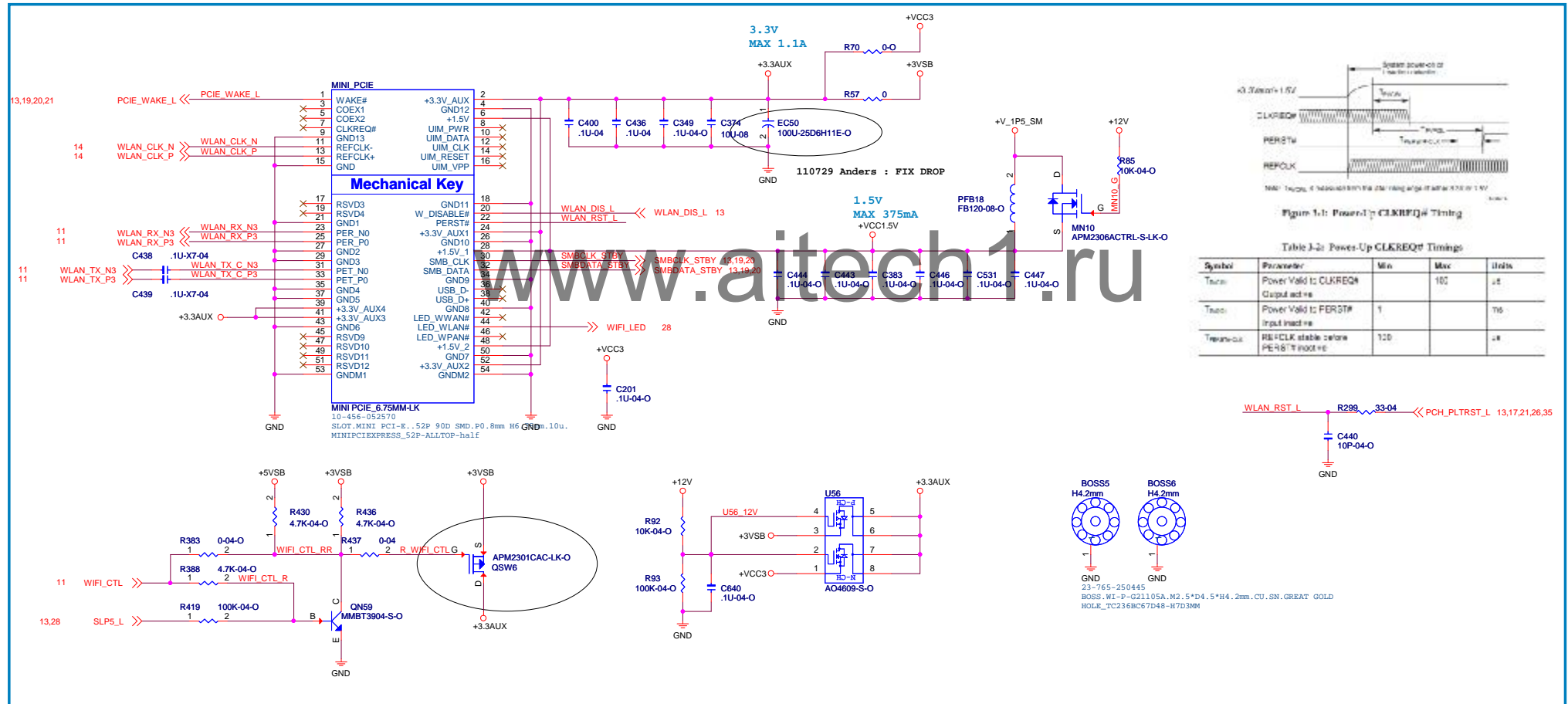


Slot - PCI-EX16/PCI-EX1		
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HDMI+USB CONNECTOR



MINI PCI-E Wireless Card Slot

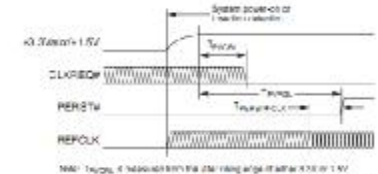
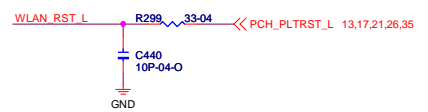


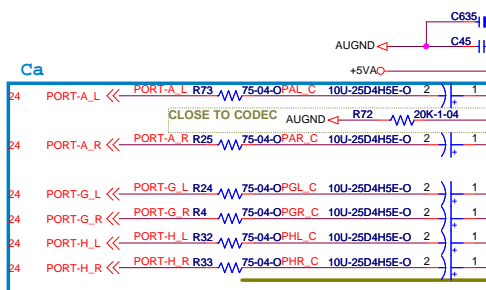
Figure 1-1: Power-Up CLKREQ# Timing

Table 1-2: Power-Up CLKREQ# Timings

Symbol	Parameter	Min	Max	Units
T _{tr}	Power Vdd to CLKREQ# Input active	100		ns
T _{tr}	Power Vdd to PERST# Input inactive	1		ns
T _{tr}	PERCLK stable before PERST# inactive	100		ns

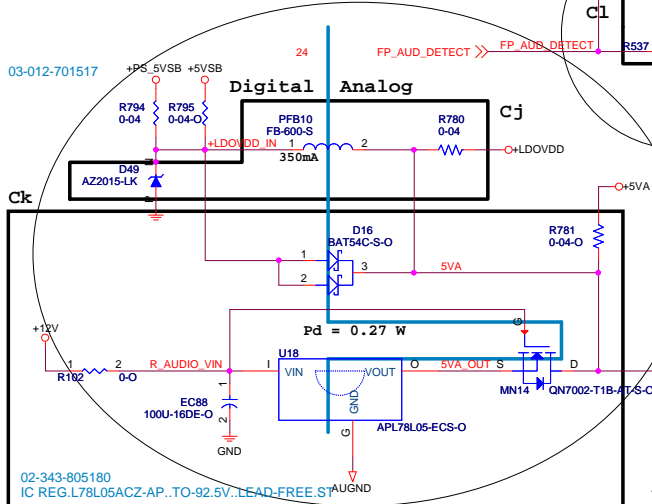


13 HDA_RST_L >> HDA_RST_L
 13 HDA_BITCLK >> HDA_BITCLK
 13 HDA_SYNC >> HDA_SYNC
 13 HDA_SDIN0 >> HDA_SDIN0
 13 HDA_SDOUT << HDA_SDOUT



GPIO(front panel detection) select table

	ALC892	ALC892S-VC	ALC662-VC	ALC662-VD
PIN-2	GPIO3/SPDIF-OUT2	SPDIF-CUT2	GPIO0	GPIO0
PIN-3	REGREF	GPIO0	GPIO1	REGREF
PIN-4	GPIO0	GPIO0	DVSS	GPIO1



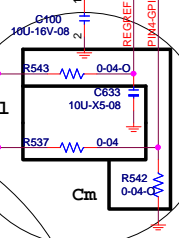
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 IC REG.L78L05ACZ-AP..TO-92.5V..LEAD-FREE.S

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Analog

Digital

Cd



110712 Anders:colay ALC662-VC

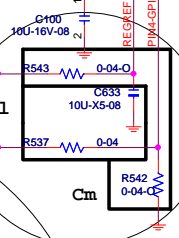
5V Max: 38 mA

AUGND
 AUGND
 AUGND
 AUGND

Analog

Digital

Cd

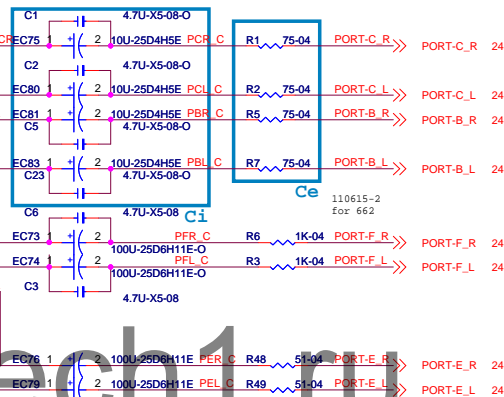


110712 Anders:colay ALC662-VC

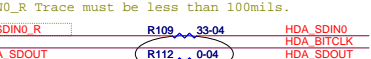
5V Max: 38 mA

AUGND
 AUGND
 AUGND
 AUGND

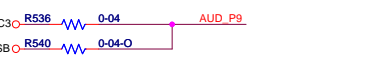
use 75 ohm for ESD,retasking 75,only output 75,
 only input 1K.



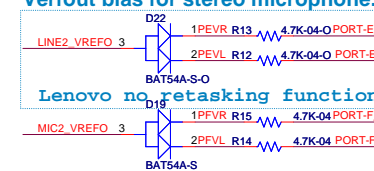
Layout Note:
 HDA_SDIN0_R Trace must be less than 100mils.



110726 Anders: FOR SI

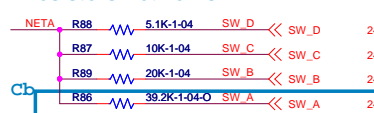


Verfourt bias for stereo microphone.



Placement near to codec

Resistors Networks



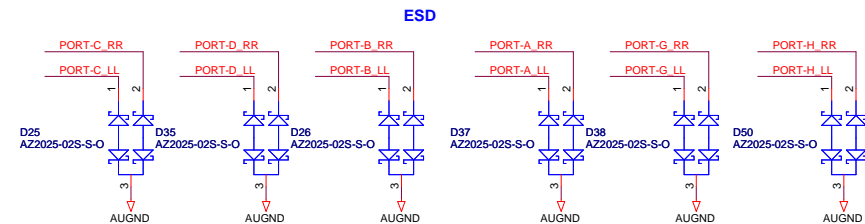
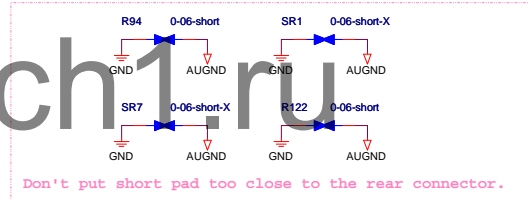
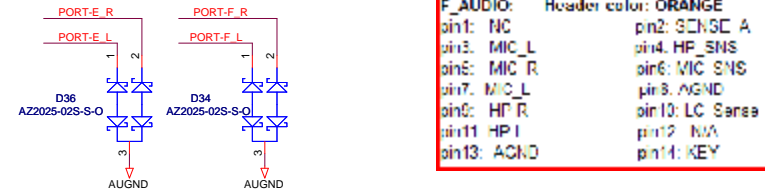
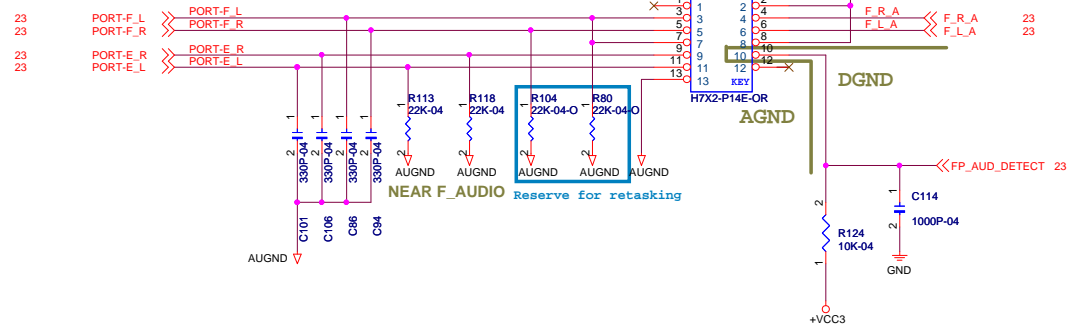
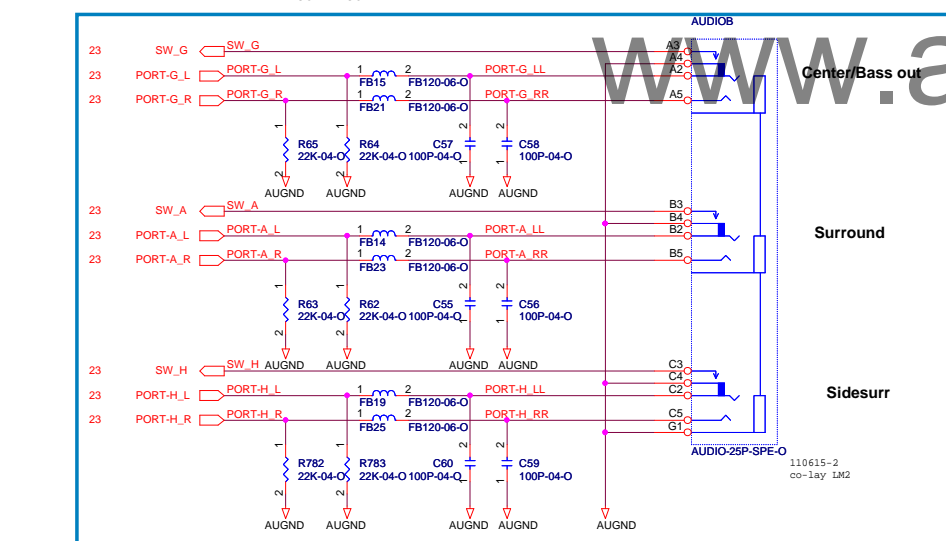
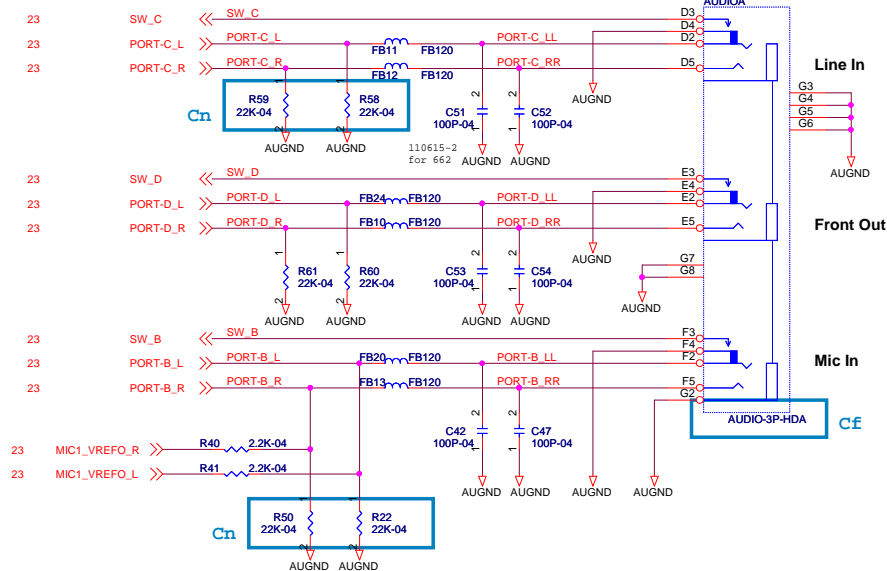
Placement near to codec

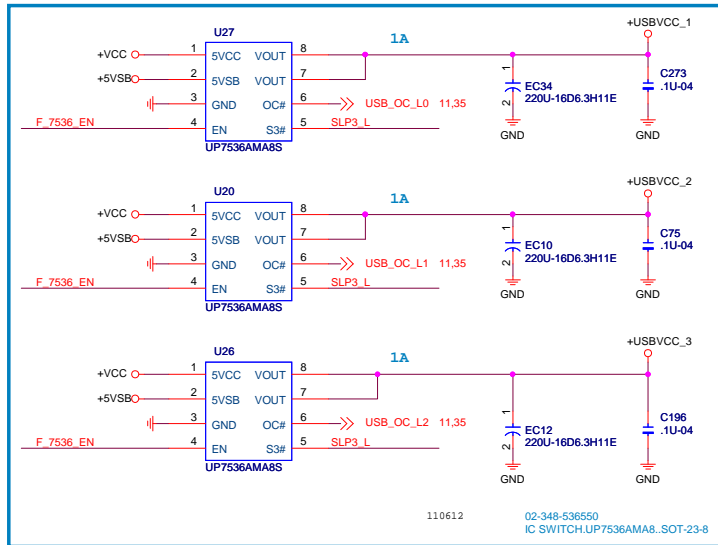
* default

	ALC892	ALC662
Ca	V	X
Cb	V	X
Cc	V	X
Cd	ALC892-CGS	ALC662-VD-GR
Ce	1K-04	75-04
Cf	AUDIO-25P	AUDIO-3P-HDA
Cg	V	X
Ci	4.7U-X5-08	10U-25D4H5E
Cn	X	V

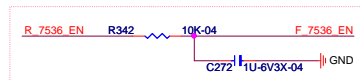
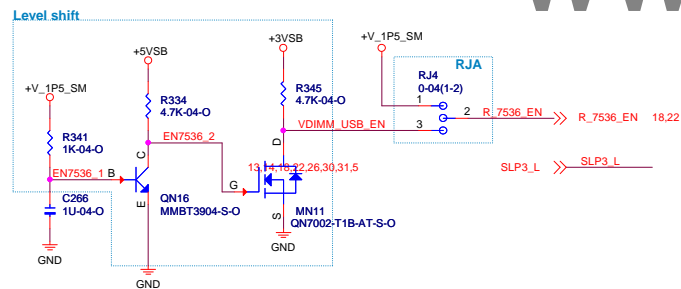
* default

	Internal LDO	External LDO
Cj	V	X
Ck	X	V
C1	V	X
Cm	X	V

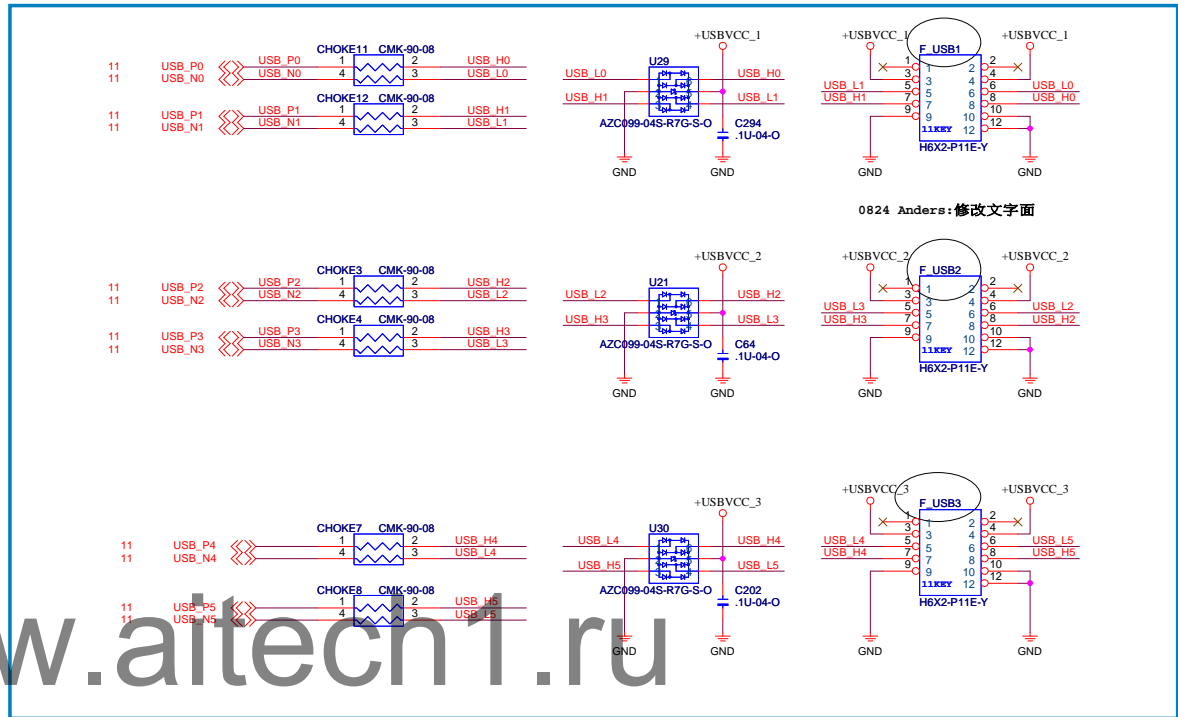
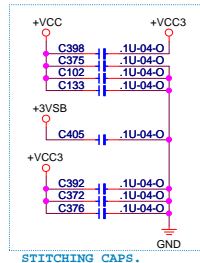




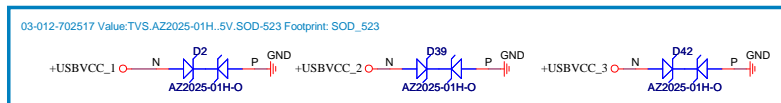
USB2.0 POWER CIRCUIT



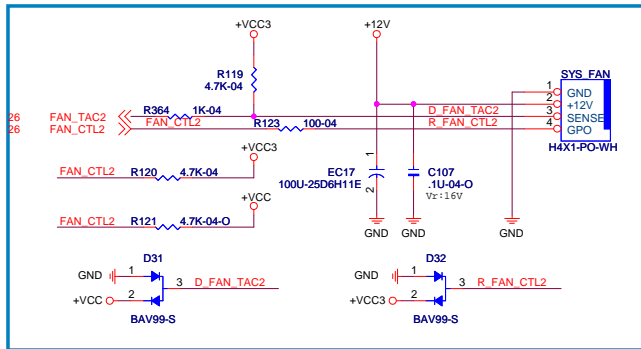
uP7536 Enable use	Level shift	RJA	RJB	S4/S5 USB_5V_DUAL	Customer
VDIMM	N A	0ohm (1-2)	N A	0 Volt	Lenovo S4/S5 w/o USB_5V_DUAL
VDIMM level shift (3.3V)	Stuff	0ohm (2-3)	N A	0 Volt	



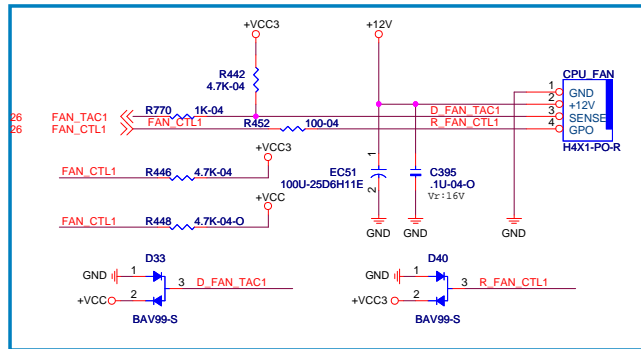
FRONT SIDE 4 PORTS USB2.0 Header



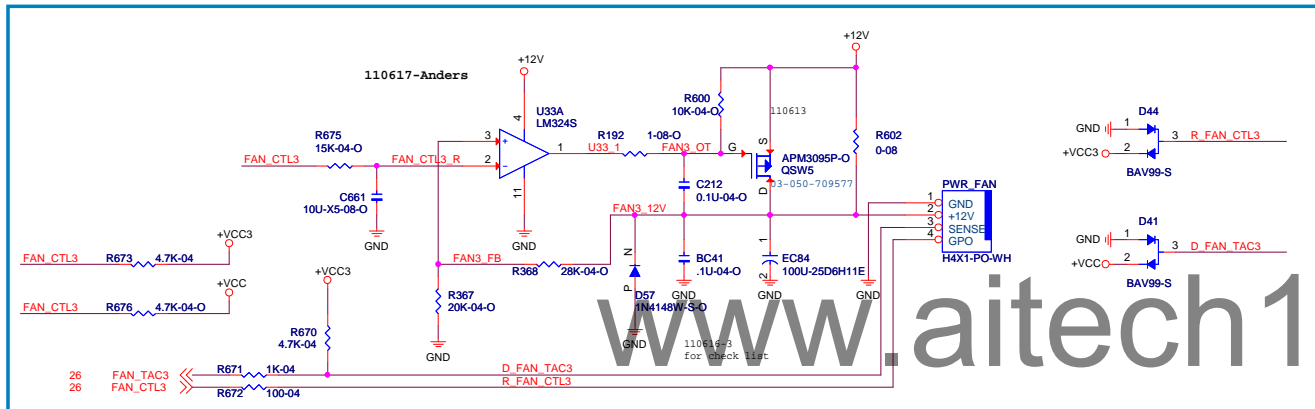
USB Header Power ESD protection diode.



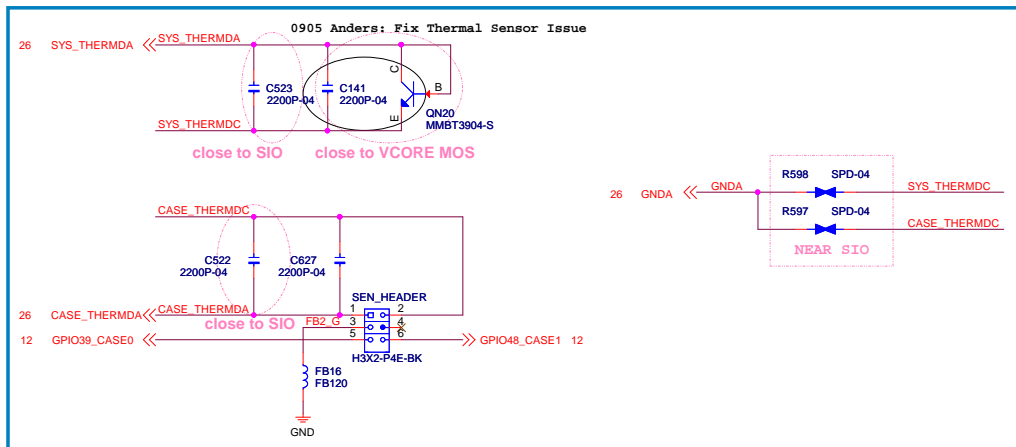
SYS FAN 4-PIN Circuit



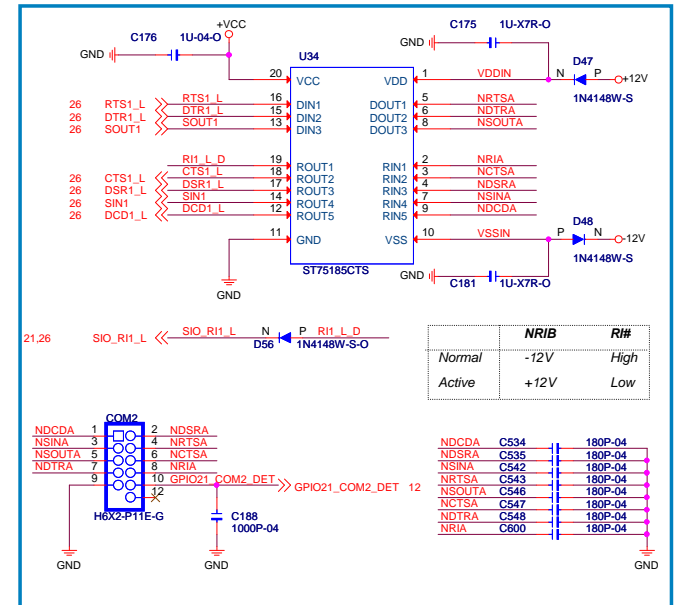
CPU FAN 4-PIN Circuit



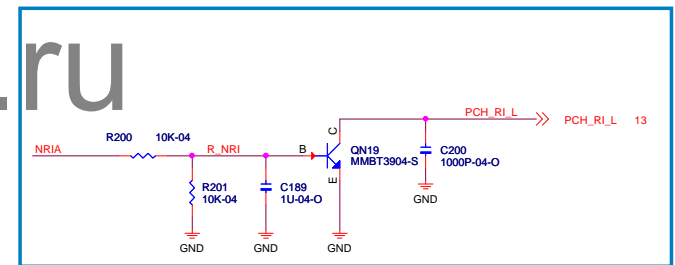
PWR FAN 3,4 pin co-layout circuit



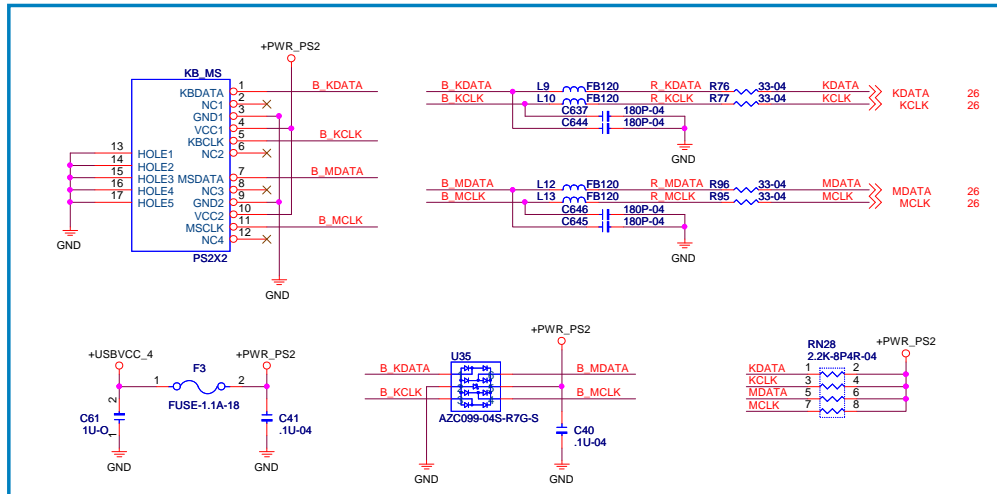
Thermal Sense



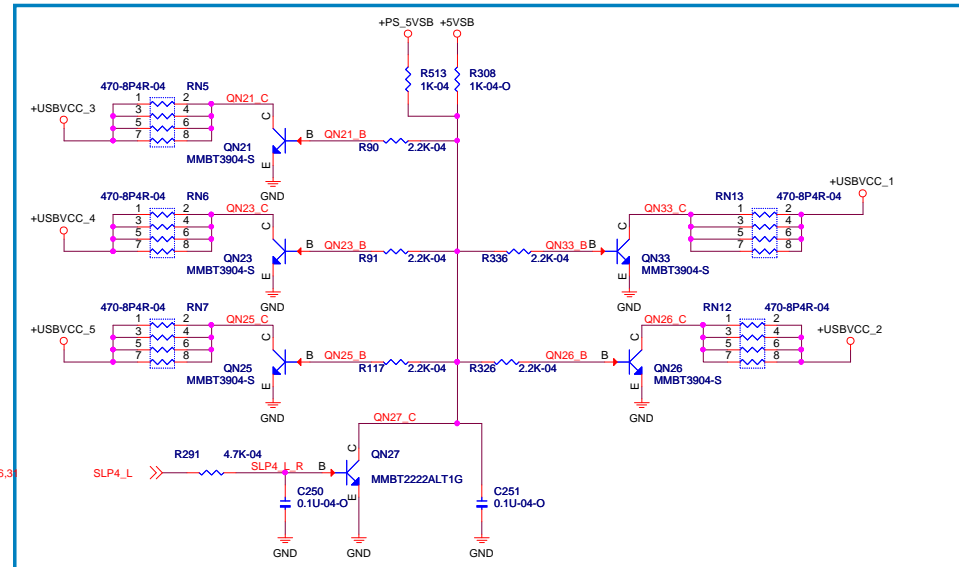
COM Header Circuit



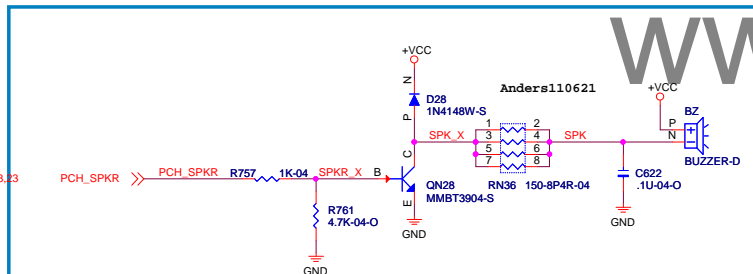
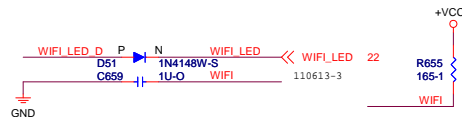
COM2 RI# Wake Up Circuit



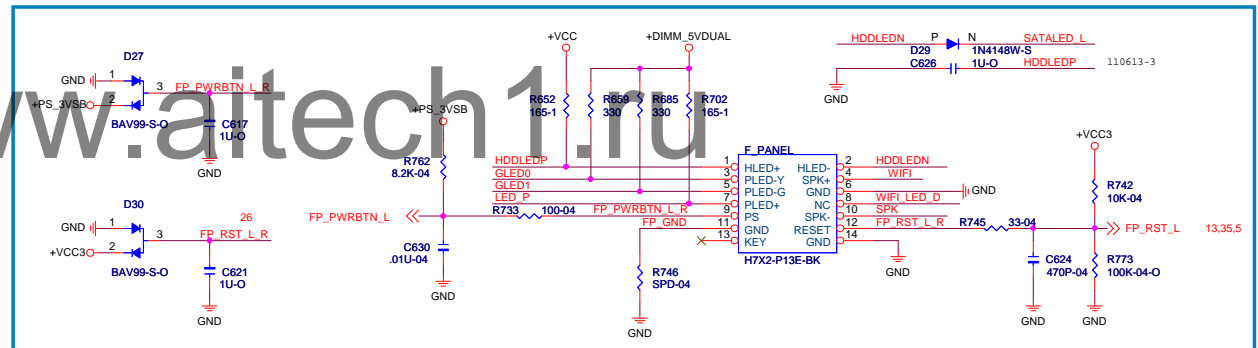
PS/2 Connector



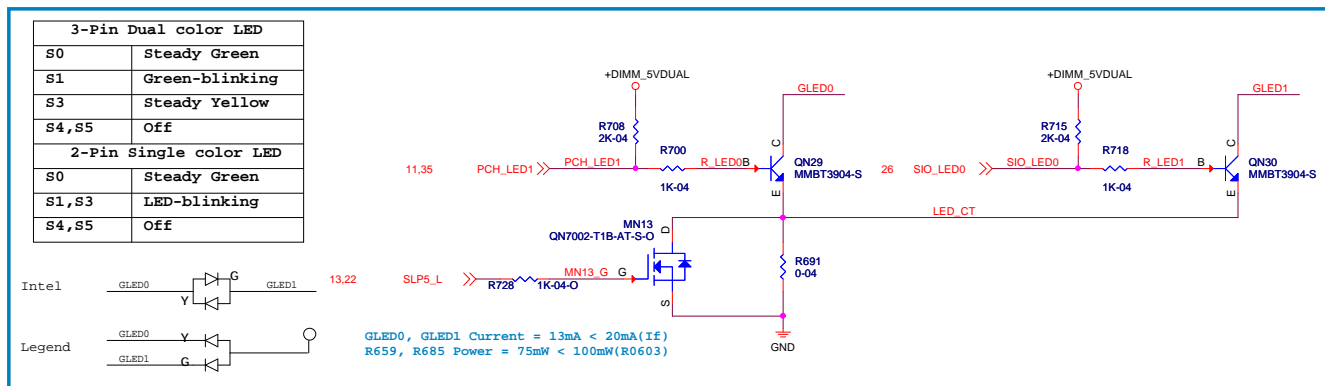
USB Discharge Circuit



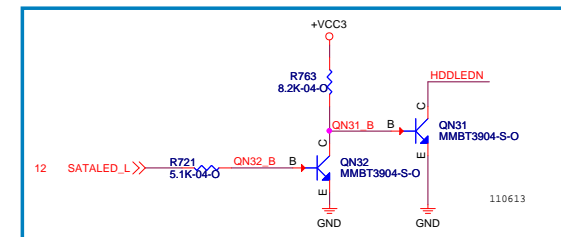
Buzzer Circuit



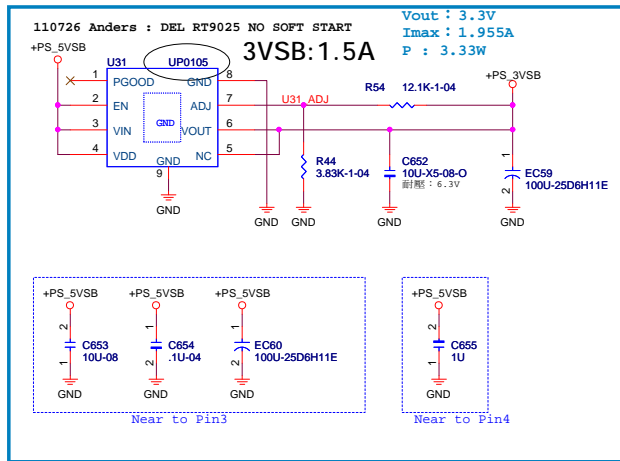
Front Panel Circuit



Front LED

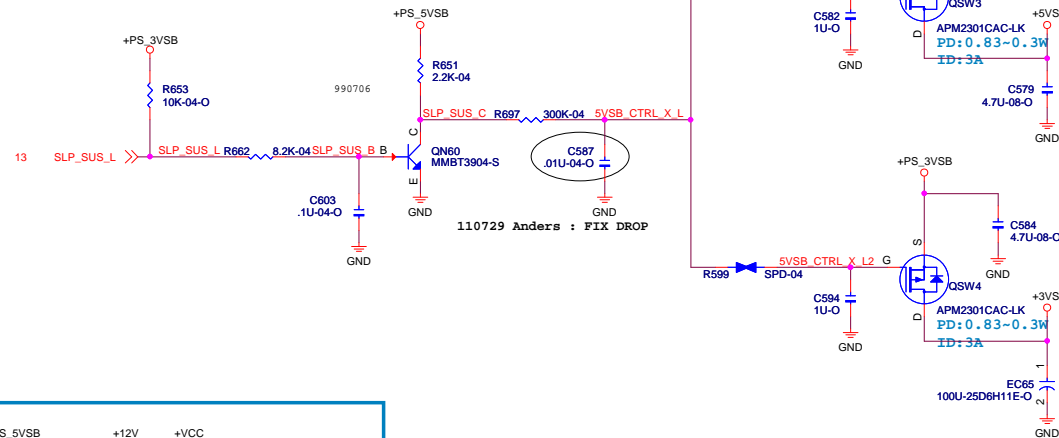


SATA LED Blink Once in Power On Issue

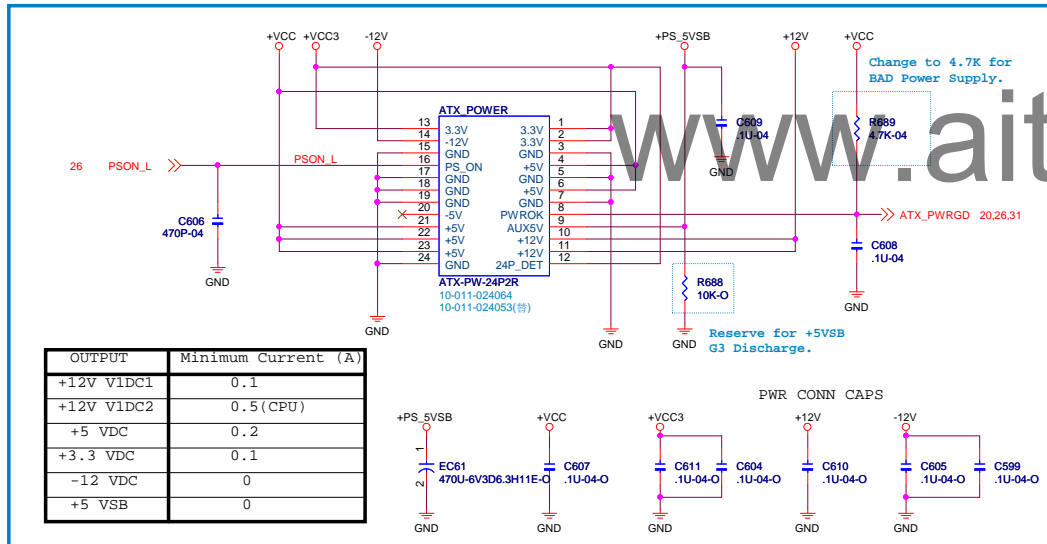


3VSB (S0):

Power Name	Current
PCH	105mA
LAN RTL8111E-VL	165mA
SIO IT8772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	1.1A
Total Current	0.28 + 2.6 = 2.88A



03-050-530179
MOSFET P-CH.APM2301CAC..
Vds=20V.Vgs=12V.Id=3A.Rds(on)=70m OHM.
SOT-23-3....LEAD-FREE(RoHS)ANPEC
03-050-540226(替)



OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5 (CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0

ATX Power 24PIN

BuP Lot6 2013 0.5W:

PWR STATE	+5VSB Source
S0	+PS_5VSB
S3	+PS_5VSB
S4	OFF
S5	OFF



Layout Note:
Close to ATX 24P2R Connector.



Elitegroup Computer Systems

Title DC/DC 3VDUAL

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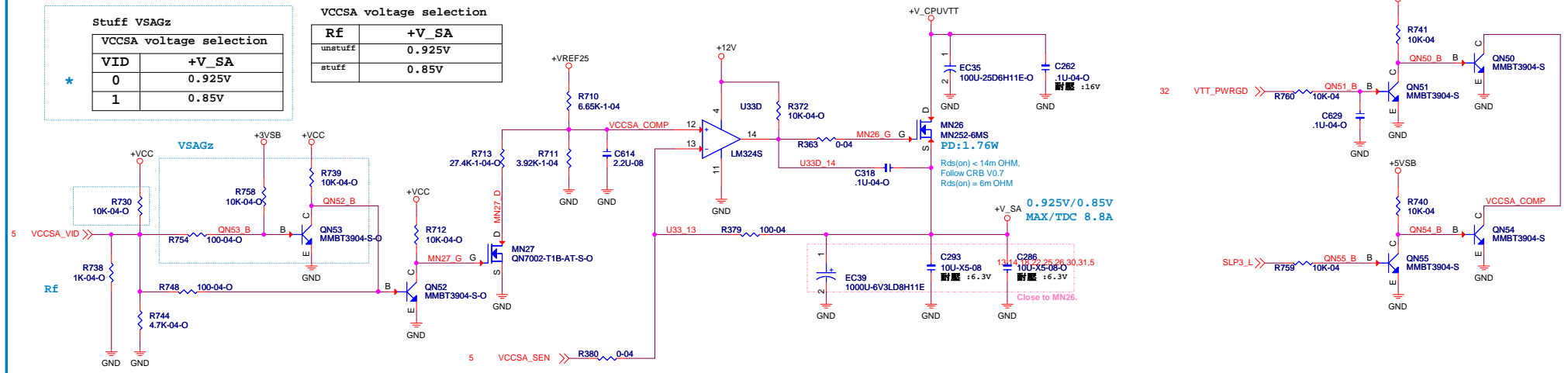
Rev 1.0

★

Stuff VSAGz

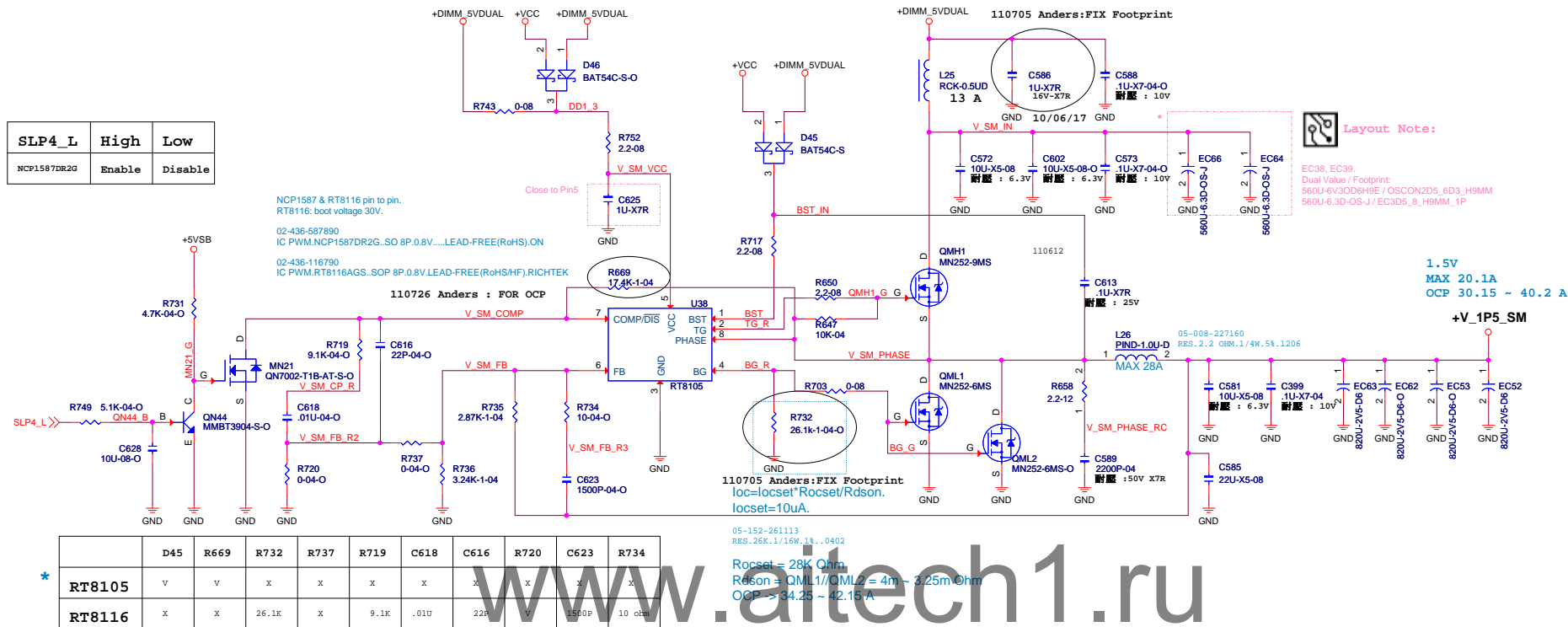
VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

VCCSA voltage selection	
Rf	+V_SA
unstuff	0.925V
stuff	0.85V



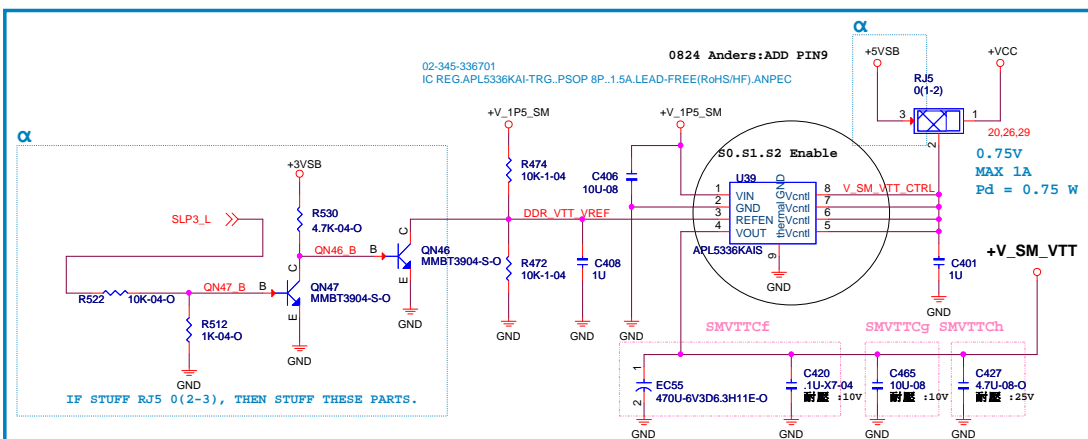
VREF25
02-348-431705
Value:IC REG.APL1431AAI-TRL..SOT-23..2.5V
Footprint: SOT23_RAC_Z_2

SLP4_L	High	Low
NCP1587DR2G	Enable	Disable



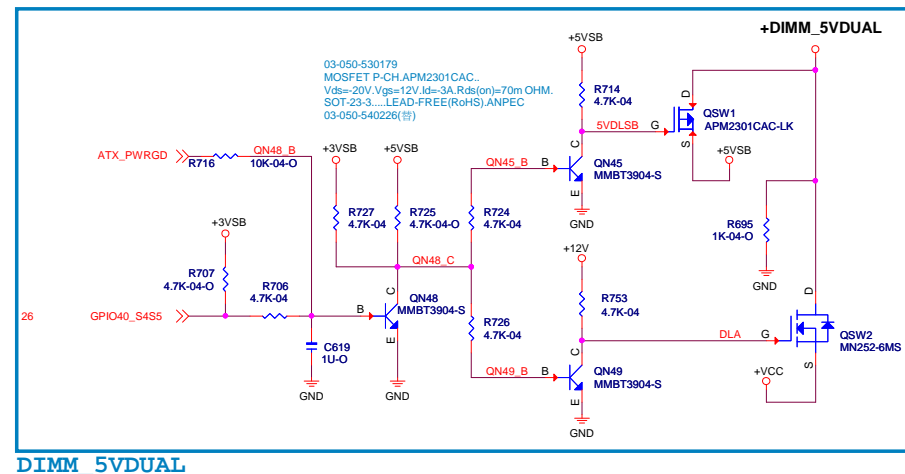
	D45	R669	R732	R737	R719	C618	C616	R720	C623	R734
RT8105	V	V	X	X	X	X	X	X	X	X
RT8116	X	X	26.1K	X	9.1K	.01U	22P	Y	1500P	10 ohm

VDIMM

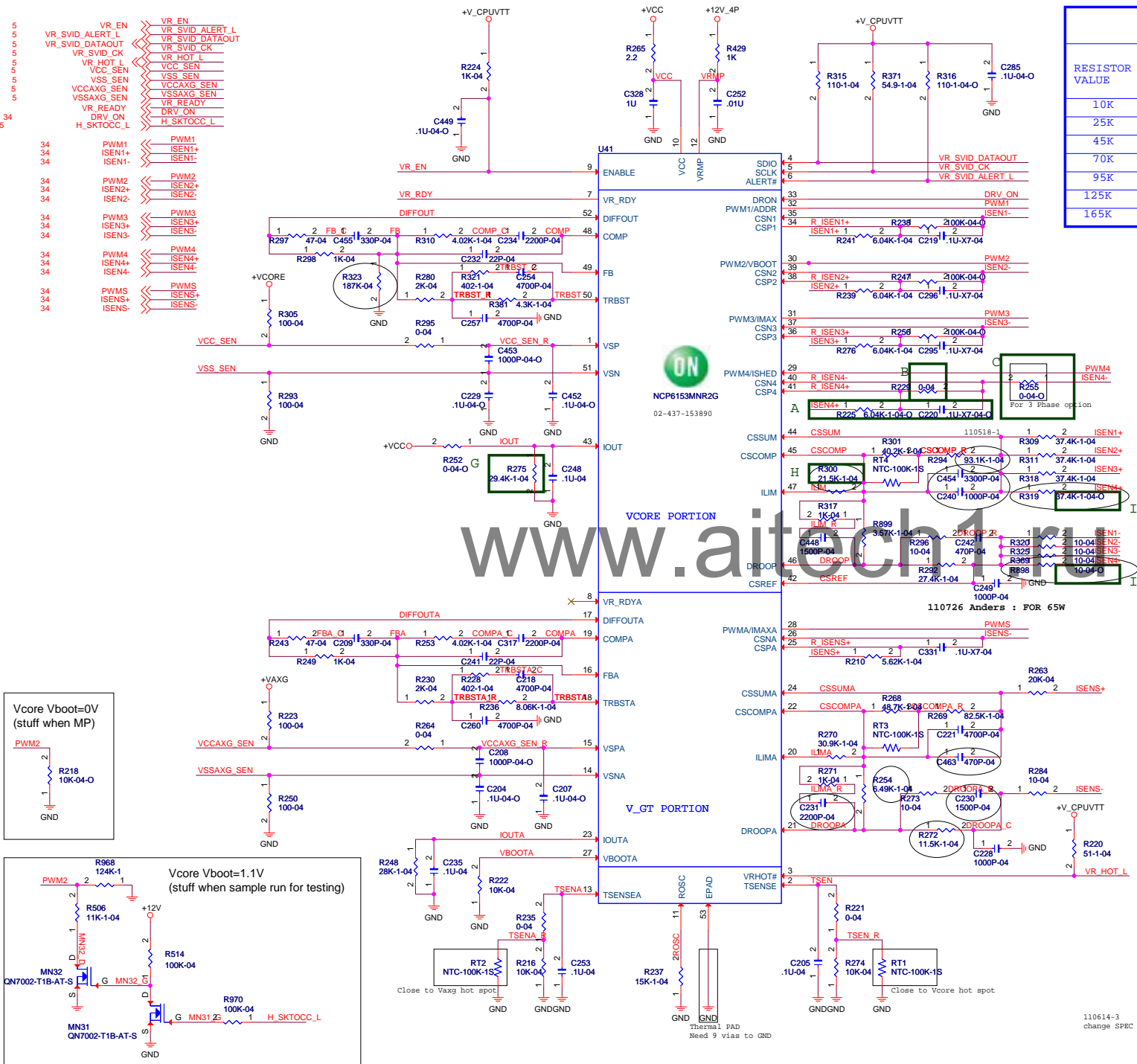


Layout Note:
SMVTTcf close to U39 Pin4.
SMVTTcg are between Channel A & B.
SMVTTCh are between Channel A & CPU.

DDR_VTT

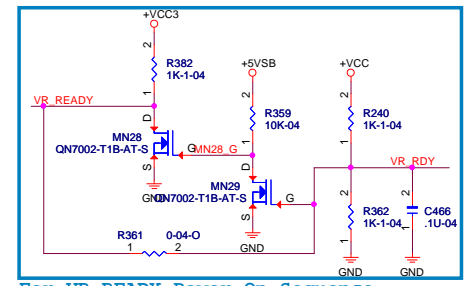
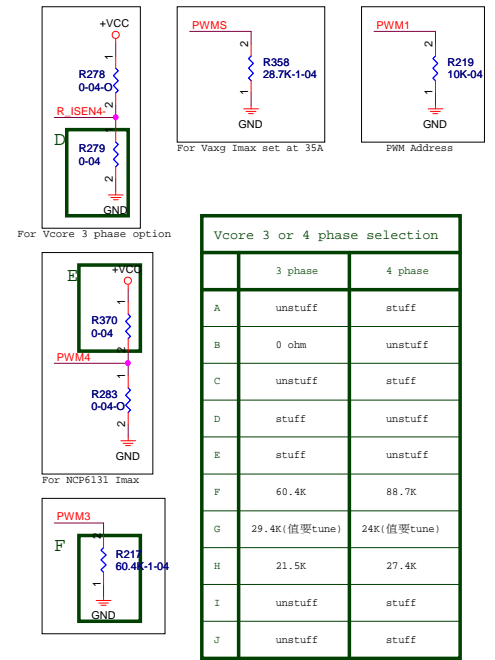


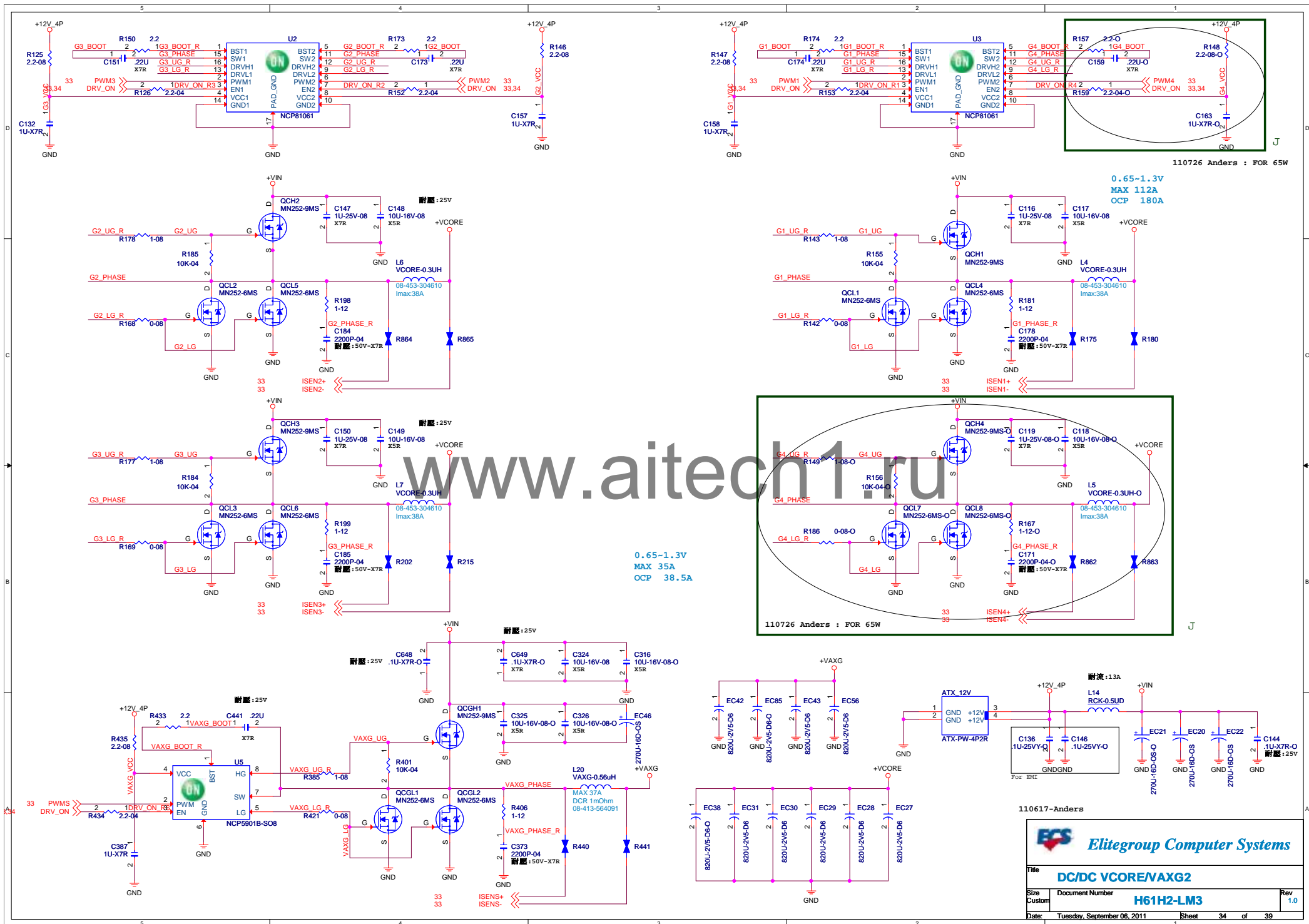
DIMM 5VDUAL

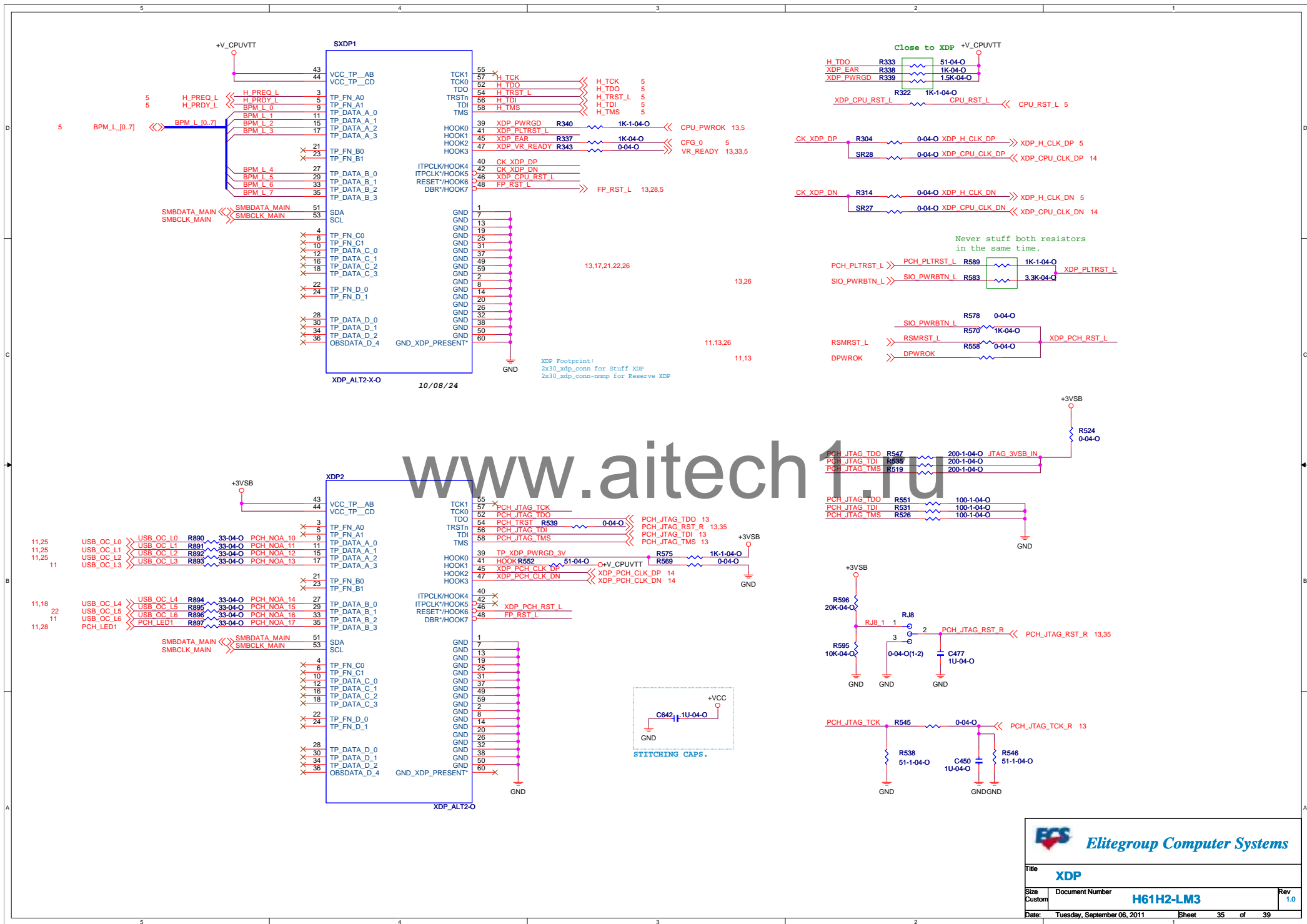


PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR Vcore RAIL	SVID ADDRESS FOR V _{GT} RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.9V
45K	1V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V







PCH Strap Pin

Pin Name	Usage	Default Status
SPKR	No Reboot	20K internal pull-down , No Reboot Mode with TCO Disabled:
INIT3_3V#	Reserved	20K internal pull-up , intend for Firmware Hub.
GNT[3]#/GPIO[55]	Disable Top-Block Swap	20K internal pull-up , "topblock swap" mode Disable
INTVRMEN	Enable Integrated 1.05V VRM	Need External Pull-up , Integrated 1.05V VRM Enable
GNT1# /GPIO51	Boot BIOS Strap bit [1] BBS[1]	20K internal pull-up , The default flash selection is the SPI flash.All
SATA1GP / GPIO19	Boot BIOS Strap bit[0] BBS[0]	20K internal pull-up , The default flash selection is the SPI flash.All
HDA_SDO	Flash Descriptor Security Override/ ME	Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default)
DF_TV5	Enable DMI termination voltage	This signal has a weak internal pull-down.
GPIO28	Eable On-Die PLL Voltage Regulator	The On-Die PLL voltage regulator is enabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select 1.8V	20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	Disable TLS Confidentiality	Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.

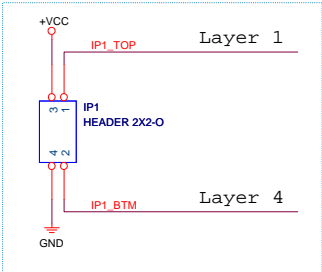
SIO Strap Pin

Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP(default)
Pin-23		0 *	DSW
JP2	WDT_EN	1 *	Disable WDT to reset PWROK(default)
Pin-57		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1 *	EC Index 6Bh/73h default = 80h
Pin-59		0	EC Index 6Bh/73h default = 00h
JP4	K8PWR_EN	1 *	Disable K8 Power Sequence(default)
Pin-61		0	Enable K8 Power Sequence

Note:
If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

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Impedance Test Header



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ATX P/S WITH 1A STBY CURRENT					
5VSB	5V	3.3V	12V	-12V	
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	

ATX4P
12V
+/-5%

Switching ISL6363 4+1 phases

Vcore:0.65~1.3V 112Amax

Vauxg:0.65~1.3V 35Amax

Switching ISL95870B 1 phase

V_CPU_VTT:1.05V 17Amax

Linear LM324

VCC_SA:0.925V(0.85V) 8.8Amax

Switching NCP1587

V_DIMM:1.5V 20.1Amax

DDR3 DIMM 1333MHz (2)	
VDDQ	7A_S0 0.5A_S3
V_SM_VTT	1.0A_S0

LDO APL5336

Linear LM324

PCH_CORE:1.05V 7.61Amax

Intel Sandy Bridge CPU			
VCCP	VID 0.65~1.3V	85A	
VAXG	VID 0.65~1.3V	25A	
VTT	1.05V(1V)	8.5A	
VCC_SA	0.925V(0.85V)	8.8A	
VCCPLL	1.8V	1A	
VDDQ	1.5V	4.5A	

Fans * 3
12V_200mA

SPI
VCC3_30mA

CRT
VCC_1A fuse

HDMI
VCC3_0.5A fuse x 1

Intel Cougar Point (TDP 5.5W)			
V_PROC_IO	1.05V	1mA	
VccDMI	1.05V	0.057A	
VccCORE	1.05V	2.1A	
VccIO	1.05V	3.8A	
VccADPLLA	1.05V	0.08A	
VccADPLLB	1.05V	0.08A	
VccCLKDMI	1.05V	0.08A	
VccSSC	1.05V	0.105A	
VccDIFFCLKN	1.05V	0.055A	
VccASW (ME)	1.05V	1.31A	
VccDFTerm	1.8V	0.002A	
VccVRM	1.8V	0.175A	
Vcc3_3	3.3V	0.267A	
VccADAC	3.3V	0.068A	
VccSPI	3.3V	0.02A	
VccDSW3_3	3.3V	0.002A	
VccSUS3_3	3.3V	0.097A	
VccSUSHDA	3.3V	0.01A	
VccRTC	3.3V	6uA(G3)	
V5REF	5V	1mA	
V5REF_SUS	5V	1mA	

Battery
3V

LAN Realtek RTL8111F-CG		
VDD3P3	3.3V	70mA
VDD1P05	1V	300mA
CTRL1P05 internal LVR Output		

SUPER I/O IT8775EX		
3VSB	3.3V	6mA
VCC3	3.3V	6mA
BAT 3.3V	3.3V	1uA

AUDIO ALC662-VD		
DVDD 3.3V	3.3V	11mA
AVDD	5V	42mA
Internal LDO Output		

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Non AMT:
VccASW(ME) short to V1P05_PCH

Linear LM324

V_SFB:1.8V 1.17Amax

Not support DSW mode:
VccDSW short to 3VSB

Resistor

+VDD33
+AVDD33

5V DUAL Switch IC UP7536

USB_5V

X16 PCIE Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

Total 1 Slot

X1 PCIE Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

Total 3 Slots

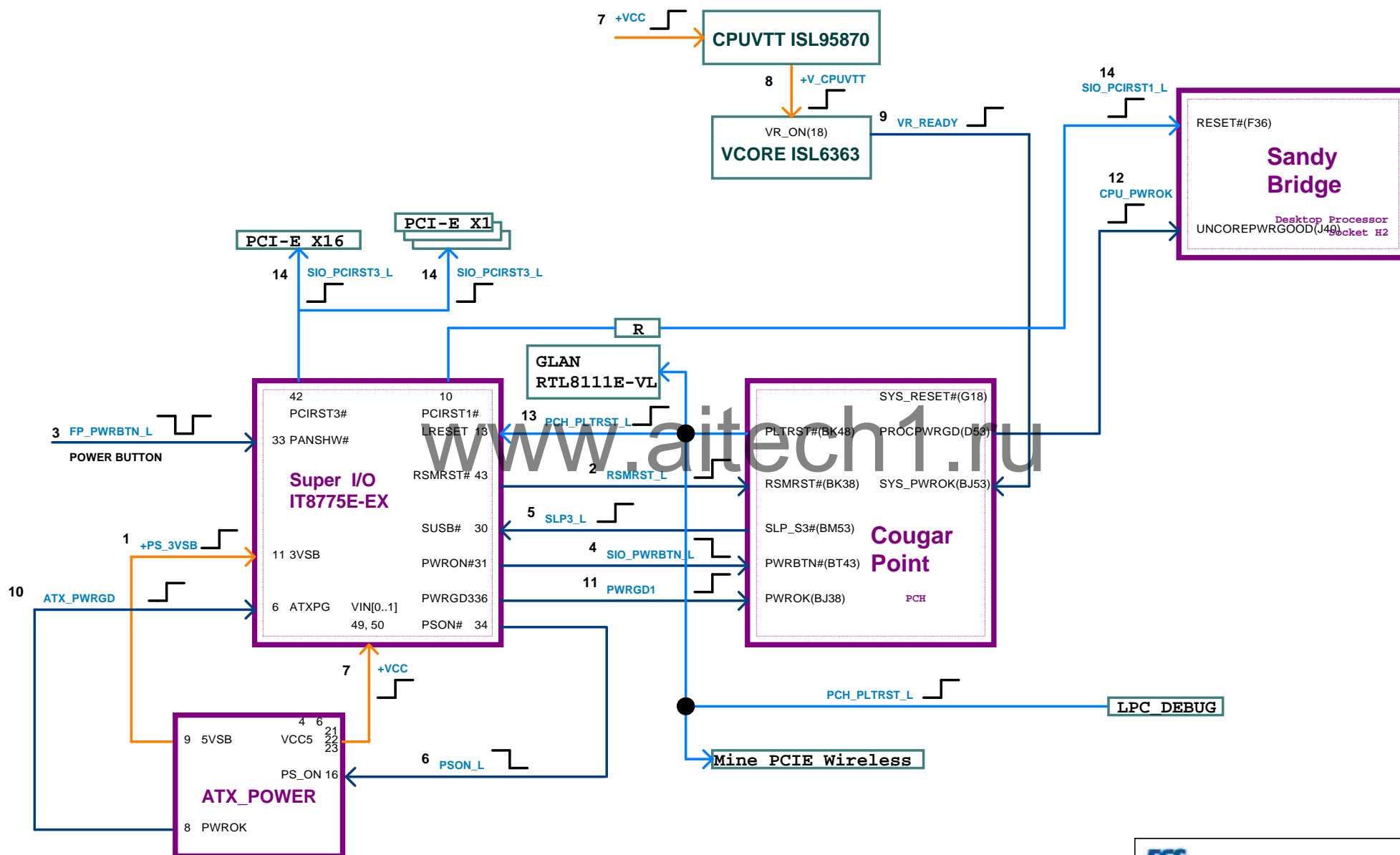
MINE PCIE Slot per	
3.3Vaux	1.1A(S0)
1.5V	375mA(S0)

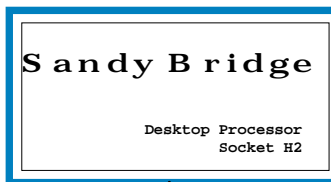
Total 1 Slot

USB20 X6 Header	
VDD	5V Dual
3.0A	

USB20 X4 IO	
VDD	5V Dual
2.0A	

PS/2	
5V Dual	275mA





CK_DIMM_A_[3:0]_H/L

DDR3 Channel A

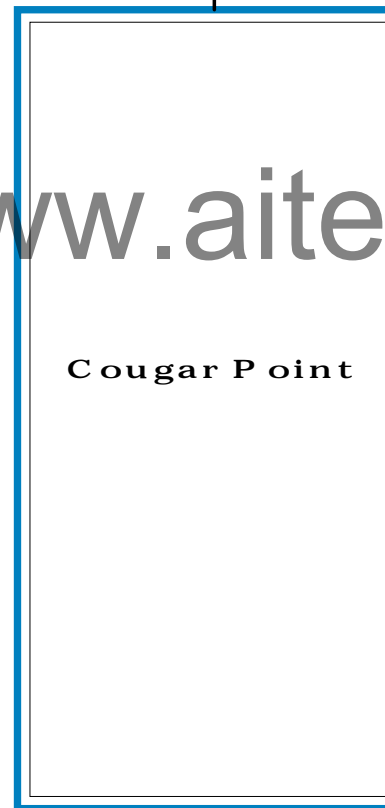
DDR3

1333MHz/1066MHz

CK_DIMM_B_[3:0]_H/L

DDR3 Channel B

CK_CPU_100M_P/N



PEX16_100M_P/N

PCI-E X16

PEX1[A..C]_100M_P/N

PCI-E X1

WLAN_CLK_P/N

Mini PCIE Wireless

GLAN_CLK_P/N

LAN
RTL8111E-VL

XTL 25M

PCI_33M_FB

LDG33M

LPC_DEBUG

SIO33M

SIO:

SIO48M

IT8775E-EX

XTL 32.768K

XTL 25M



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Clock Distribution

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